Abstract

DEMARCO, STEPHEN CHRISTOPHER The Architecture, Design, and Electromagnetic/Thermal Modeling of a Retinal Prosthesis to Benefit the Profoundly Blind (Under the direction of Dr. Wentai Liu and Dr. Gianluca Lazzi).

This dissertation describes the design and study of a retinal prosthesis for individuals who have suffered loss of vision from degeneration of the outer retinal layer. Retinitis pigmentosa and age-related macular degeneration lead to blindness through progressive loss of retinal photoreceptors. Acute experiments reveal that direct electrical stimulation of remaining ganglion cells in degenerate retina elicits localized visual percepts in blind RP/AMD patients. This motivates research toward the development of a retinal prosthesis system involving an implantable stimulator microchip to compensate the defective photoreceptor layer. This retinal prosthesis under development jointly at North Carolina State University and the Wilmer Eye Institute at Johns Hopkins University may recover a limited sense of vision, compatible with mobility and perhaps even reading large scale print.

Many prostheses do not reside fully inside the body, but rather consist of an implantable stimulation unit and a linked exterior wearable portion. This is motivated by the desire to have a simpler implant with ease of upgrading signal processing and other aspects of the exterior unit without incurring re-entrant surgery. Although percutaneous (wired) connections between external and internal units have been used in earlier developments, the transcutaneous (wireless) link is the method of choice due to reduced mechanical tethering on the implant and lower risk of infection. Thus, there is a need in the retinal prosthesis to deliver power to the implant and support high-speed bi-directional communication with the stimulus electronics in a wireless fashion. Therefore, the current progress in the common types of non-invasive connections to bio-implants is reviewed as it relates to the power and communication needs of prostheses.

The extraocular master controller of the prosthesis discussed here is a hardwarereconfigurable unit based on FPGA technology and is described in the context of its role in image processing and producing real-time instructions for the implantable micro-stimulator IC. When placed in an enclosure along with NCSU's *Retina-3.5* packaged microchip, the controller provides a backpack stimulator which supports twenty-five simultaneous biphasic-pulse current outputs for extraocular, trans-sceral, retinal stimulation. Thus, the same extraocular hardware designed to support chronic human implants can also be adapted for use in animal experiments and can be attached to an animal's torso to operate in a stimulatory fashion autonomously.

NCSU's most recent implantable retinal-stimulator IC is described in detail. The device is designed to provide electrical stimulation to the remaining ganglion cells of post-degenerative retina in blind RP and AMD patients. The IC contains sixty stimulus circuits providing biphasic current pulses to sixty unmultiplexed outputs and is designed to drive a separate micro-fabricated electrode array with unmultiplexed biphasic stimulation currents up to 600μ A in amplitude. Pulse amplitudes and timing parameters including pulse widths, interphase delay, and stimulation frequency can be programmed in real-time in order to manipulate visual percepts. Power dissipation in the stimulator IC is characterized through circuit simulation and verified with experimental measurement. Also described is a design technique to significantly reduce the on-chip area of the stimulus circuits. This yields more output channels per chip area, thereby raising the stimulation resolution for bio-implants.

Temperature elevation in the eye and surrounding head tissues associated with with the retinal prosthesis is studied. Losses in the tissues occur due to the permeating electric field arising from inductive (coil-based) coupling for power and data telemetry with the implant. Further losses occur from power dissipation in the implanted micro-stimulator IC. These two sources of power account for heating in the tissues and are studied through numerical simulation of the electromagnetic and thermal processes. A high-resolution 2D human head and eye model is developed at 0.25mm spatial resolution with associated dielectric and thermal properties suitable for numerical simulations. The Finite Difference Time domain method (FDTD) with material independent absorbing boundary conditions is used to predict with high detail the specific absorption rate (SAR) induced from electromagnetic exposure to inductive telemetry with the implant for wireless power and data transfer. A highly detailed heating pattern in the eye tissues due to the SAR and power dissipation in the implanted stimulator is computed using a time-domain numerical implementation of the bioheat equation.

The Architecture, Design, and Electromagnetic and Thermal Modeling of a Retinal Prosthesis to Benefit the Visually Impaired

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Biography

Stephen C. DeMarco was born on October 11, 1971 in Fairmont, WVa. He graduated from Clinton High School of North Carolina in 1989. He received the B.S. degree in Computer Engineering (Summa Cum Laude) from North Carolina State University in 1994 and the M.S. degree in Computer Engineering from North Carolina State University in 1996. In December 2001, he earned the Ph.D. degree in Computer Engineering at North Carolina State University.

His research is in the areas of analog/digital/mixed-mode circuit design, VLSI, FPGA's (Field Programmable Gate Arrays), and computer vision/image-processing applicable to retinal prosthesis development. The project which he represents is a joint research effort between ophthalmologists/surgeons and researchers at Johns-Hopkins University and electrical engineers/researchers at North Carolina State University. The goal is the development of a chronic retinal prosthesis implant to recover limited vision to people who are blind due to outer retinal degeneration caused primarily by the two diseases Retinitis Pigmentosa and Age-Related Macular degeneration.

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Chapter 1

Introduction

1.1 Motivation

The use of electrical stimulation to recover lost bodily functions has been pursued for nearly 50 years [1], [2]. As the integrated circuit had not been developed at this time [3], it was inconceivable that an electronic prosthesis of any kind could be developed for rehabilitation and recovery of lost bodily function which would also be of a size suitable for implantation. Since that time, the capabilities and miniaturization of integrated circuit technology has greatly progressed and motivated rapid progress in the development of implantable electrical stimulation devices. From this research and development have emerged electronic prostheses for functional neuromuscular stimulation [4], [5], control of internal organs [6] and sensory organs such as the well researched cochlear prosthesis [7]–[11]. The success in recovering a limited sense of hearing has now encouraged several groups to investigate how this technology could be adapted to function as prostheses for the visually impaired.

Age Related Macular Degeneration (AMD) and Retinitis Pigmentosa (RP), among the leading causes of blindness [12], effect over 10 million people worldwide through progressive photoreceptor loss (rod/cones) in the retina [13]. The photoreceptor cells in a healthy retina initiate a neural signal in response to incident light. This neural signal is further processed by bipolar and ganglion cells of the inner retina prior to delivery to higher processing areas in the visual cortex. Retinal photoreceptors are almost completely absent in the retina of end-stage RP and AMD patients, while the bipolar cell and ganglion cells, through which the photoreceptors normally synapse, survive at higher rates in the macular region [14], [15], but to a lesser extent beyond the macula [16]. The ganglion and bipolar cells remain intact, and due to the anatomy of the retina, they are in a position where they may respond to artificially-induced electrical stimulation via an implant.

The demonstration that direct electrical stimulation of retinal ganglion cells can elicit visual perception in blind patients has been shown clinically [17], [18]. A number of acute epi-retinal electrical stimulation experiments have been conducted at the Wilmer Eye Institute at Johns Hopkins University on individuals blinded from RP and AMD [18]. Ten patients were considered and three different types of electrode arrays were explored. In one case, a patient receiving electrical stimulation from a 5×5 site electrode array of 400μ m platinum disks separated by 200μ m, correctly elicited the perception of the letter "H". This begins to establish the foundation that form vision (that is, the perception of "features", including edges and patterns) can be mentally extracted from discrete electrical stimuli. This opens the possibility of an electronic prosthesis to bypasses the defective photoreceptors.

1.2 Prosthesis structures under consideration

It is evident that there are several locations within the human visual pathway which could be electrically stimulated to elicit perception in blind patients, each with advantages and disadvantages which are discussed. The first stage encountered in the visual pathway consists of the photoreceptors (rods/cones) in the retinas outer layer, where incident light is transduced into electrical impulses to be further processed by the inner retinal layers. Visual prostheses which target electrical stimulation of the retina are classified into two types which differ according to whether the outer retina is stimulated, referred to as the sub-retinal approach, as opposed to stimulation of the inner retina, referred to as the epi-retinal approach. Contrary to either of these two forms of retinal stimulation, the optic nerve, posterior to the retina, represents another target for electrical stimulation. The final stage of the visual pathway considered for electrical stimulation by an implantable device is the cortex in the rear portion of the brain.

1.2.1 Sub-retinal approach

Serveral research efforts pursue the sub-retinal approach [19], [20] which seeks to stimulate the retina at its outer surface between the retinal pigment epithelium anterior to the choroid and the retinal photoreceptor layer. In the sub-retinal configuration, a micro-photodiode array and stimulator circuit array are designed fully integrated and form the whole of the retinal prosthesis. An attractive aspect of the sub-retinal approach is that the "active" or circuit side of the integrated circuit die faces toward the pupillary aperture, which opens the possibility that the stimulator circuit may derive its power for retinal stimulation from incident light entering the eye.

Furthermore, the retina's neural network structure is known to perform signal preprocessing on images projected optically onto its photoreceptor layer [21]–[23]. By electrically stimulating the retina from the posterior, or outer surface, the signal flow through this network may be preserved in a manner consistent with natural biological vision.

A potential disadvantage of the sub-retinal approach is that the inner-retinal placement of the micro-photo diode array and stimulator microchip may lead to retinal damage through pigment-epithelium separation or obstruction of blood flow from the choroid into the retina [24]. Furthermore, a hermetically sealed device positioned posterior to the retina with no communication mechanism with the external world does not facilitate configuration or programming of stimulation pulse parameters, such as amplitudes, pulse widths, interphase delay, and stimulation frequency, which have been found to influence the quality of perception [17], [18]. Moreover, the greater distance from any extraocular components of the prosthesis to the implant now residing at the back of the eye increases the challenge of supporting inductively coupled power (if the micro-photodiode array proves insufficient for generating adequate power) and communication initiated extraocularly, owing to weaker coil coupling over the greater distance.

1.2.2 Epi-retinal approach

Several research groups have adopted the epi-retinal approach [24]–[32] which, in contrast to the sub-retinal arrangement, seeks to stimulate the retina from the inner surface, adjacent to the ganglion cell and axonal layers. A generally common characteristic among the epi-retinal development efforts is the partitioning of the system into an intraocular unit, consisting of the retinal stimulator, and an extraocular unit, providing front-end signal processing, which in being external now facilitates easier refinement or upgrading. This partitioning becomes necessary when the surgical placement and orientation of the implant exacerbates the delivery of power and/or video input, especially when the active side of the integrated circuit faces inwards towards the retinal surface. The two units are typically coupled with a wireless power and data telemetry mechanism, which can take several forms. Some researchers are studying optical power and telemetry based a laser diode [33], while others are considering inductively coupled power and data telemetry [30]–[32]. Researchers also report the development of a hybrid prosthesis design in which neurons are cultured

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onto an electrode substrate to be used in the epi-retinal arrangement [28], [29]. Power is provided extraocularly, while video input is captured from an intraocular microphotodiode array, rather that telemetered wirelessly from the outside.

The strengths of the epi-retinal approach derive from delegating most or all of the image acquisition and processing algorithms to an extraocular position. Excluding all components except for the receiver coil, power/data recovery, and the retinal stimulator, results in a smaller, lower-power intraocular unit, while also preserving the flexibility of upgrading the image processing algorithms without re-entrant surgery. However, by stimulating the ganglion cells from the vitreo-retinal side, the natural image processing in the retina's neural network is now largely bypassed unlike the sub-retinal approach [24]. Accordingly, the extraocular unit may now be required to emulate this such that retinal stimulation is delivered which is most similar to the "natural" synaptic input [21]. Efforts are underway to integrate this retinal functionality into an epi-retinal design by emulating ganglion cell receptive-fields in an extraocular signal processor [34], [35]. Another potential disadvantage of the epi-retinal approach relates to mechanical anchoring of the implant and long term stability of the interface at the inner retinal surface. Unlike the sub-retinal approach where the implant may receive some mechanical support from the tissues posterior to the retina [36], an epi-retinal placement of the stimulator at the vitreo-retinal surface imparts the weight and inertial forces of the implant onto the fragile retina [24], [37], which is known to be very sensitive and reactive to physical stresses, potentially leading to tears, bleeding, and detachments [38] or to cellular overgrowth potentially compromising the retinal-electrode interface [24], [39]. A proposed solution adopted by those favoring the epi-retinal approach is to anchor the integrated circuit portion of the implant including the stimulator IC at a more mechanically stable position, such as at the vitreous base [24], in the crystalline lens cavity [31], [40], or at midvitreous [41].

From here, the stimulator IC is attached to a thin-film electrode array, polyimide for instance, with embedded interconnect to route stimulation currents from the stimulator IC to the vitreo-retinal surface. The end attached to the retina provides platinum or activated iridium oxide surface electrodes and is attached to the retina with titanium tacks [42], [43], biocompatible glues [44]–[46], or *Hydrogel* [39]. This proposal reduces stress on the retina while also relocating the implant electronics away from the retinal surface to the anterior chamber, thus removing IC generated heat from the retina and also improving inductive telemetry through reduced coupling distance. However, this now introduces the challenge of manufacturing a thin-film electrode array with a high density of interconnects in a narrow width in order to be surgically implantable while remaining mechanically flexibile. A further complication is introduced as the interconnects must feedthrough the sealed implant encapsulant to make attachment with the stimulator electronics without compromising hermeticity.

Both the sub-retinal and epi-retinal approaches benefit from the close association known to exist between the placement of retinal stimulation and the localized perception within a patient's visual field. This is a direct consequence of the topography of ganglions cells [47] and remaining neuron cell-types across the retina. As a wide field of view and peripheral vision relate to the large coverage of the retina within the posterior half of the eye, the stimulation of a small retinal area is expected to elicit a restricted field of view, or "tunnel vision. Research in flexible structures based on polyimde [48] and silicon [49] may yield electrode arrays which can adapt to the retinal curvature with the possibility of stimulating a greater retinal area. However, since both current sub-retinal and epi-retinal approaches target a small area of the retina near the fovea, some limitation can be expected in developing a retinal prosthesis in this way which elicits a wide field of view. Beyond these observations, however, there is yet no conclusive evidence among these research efforts as to whether the sub-retinal or epi-retinal approaches will yield a more effective chronic retinal prosthesis.

1.2.3 Optic nerve approach

The approach of electrically stimulating the optic nerve in the pre-chiasmatic region posterior to the eye is reported in [50]. This is performed with a cylindrical cuff electrode array with disk electrodes along the inside surface, which is placed around the optic nerve near its connection with the eye [51]. The order of axonal fibers within the optic nerve bundle particularly in the region where the nerve exits the eye is generally related topographically to the location of their parent ganglion cells on the retinal surface [52]. Accordingly, fibers near the surface or the nerve connect with ganglion cells near the outer edge of the retina and fibers centrally located within the nerve attach to ganglion cells closer to the foveal/macular region. Thus, because of the analogous topographic mapping of retinal ganglions to the perceptual space, or visual field of view, the excitation of near-surface fibers in the optic nerve from the cuff electrode would be expected to elicit percepts in the outer periphery of the visual space. However, encouraging results are reported that patients experience more centrally localized perception closer to the macular region [50], [51], thus supporting the proposal of optic nerve stimulation as a viable approach to visual prostheses. Perhaps the strongest advantage of this approach is that the challenges of interfacing with the delicate retina upon a curved surface are circumvented. However, the obvious hurdles to be overcome with the optic nerve approach include delivering a sufficiently high level of spatial resolution from the cuff electrode as to be practical in a visual prosthesis [53] and achieving preferential stimulation of more centrally located nerve fibers in order to explicitly target excitation in the fovea/macular region.

1.2.4 Cortical approach

Yet another approach to visual prostheses which is receiving attention is the electrical stimulation of the visual cortex [37]–[56]. The prosthesis reported in [37], consists of a 10×10 array of 1mm penetrating electrodes fabricated in silicon with platinum tips implanted into the neural tissue beneath the outer resistive dura mater [57], [58]. The array is bonded to an electrical stimulation IC and further attached to a planar spiral inductor fabricated on thin-film polyimide which is inductively coupled to an external transmitter coil for power and data telemetry [59]. Thus, a hermetically sealed implant is completely enclosed and maintains a transcutaneous link with external signal processing electronics.

Notwithstanding that most forms of blindness involve the retina [54], perhaps the greatest potential of the cortical approach is that any defects in the visual pathway forward of the cortex are bypassed, thus greatly extending the applicability of such a prosthesis to address blindness. Whereas the sub-retinal and epi-retinal approaches target RP and AMD, the cortical approach is not limited to these two diseases, but may address any number of visual disorders. However, the need to access the brain for the implantation could be a cause for concern among patients. But, the greatest challenge to the cortical approach lies in mapping the visual space. The convenient analogous spatial relationship between the retina's cellular topography and the perceptual space is no longer preserved at the cortex, where a complex spatio-temporal mapping of the visual space occurs [24]–[60]. Accordingly, adjacent locations on the cortex when stimulated electrically do not elicit adjacent percepts in the visual space [37]. However, it is proposed in [24] that the plasticity of the brain to adapt and assimilate information presented in a non-optimal fashion from the prosthesis might prove effective despite the complex cortical mapping.

1.3 NCSU's prototype system

As indicated earlier, the prosthesis in development at NCSU and JHU is of the epiretinal type, with the receiver coil to be mounted in the lens cavity and the stimulator IC suspended from the coil at midvitreous with an attached thin-film electrode array proceeding to the vitreo-retinal surface. To justify this configuration, studies were conducted at JHU [61] following the acute electrical stimulation experiments on blind RP/AMD patients [17], [18] to determine the long-term tolerance of the retina to the electrode array placement and material composition as well as to determine the longevity of the electrode array itself within the ocular environment. Encouraging results are reported in [61] of implantation in dogs of the inactive 5×5 electrode array used in the acute human trials of [18]. After several months, no retinal detachments, infections, or extensive bleeding were found to have occurred. The MIT/Harvard group also investigated the physical response of the retina to a contacting thin-film electrode array in the rabbit eye [39]. A pre-stressed, or curved, polyimide electrode array has been developed with the intention of matching retinal curvature so as to impart minimal downward force. In this study, cortical vitreous at the retinal surface in the rabbit eye was found to be sensitive to contraction from physical stresses [39]. However, upon removal of this vitreous from the attachment area, encouraging results are reported towards securely attaching the array without imparting damaging physical stresses [39].

With confidence from these experiments that the epi-retinal approach is justifiable with respect to the electrical and mechanical issues and that success is achievable using a thin-film electrode array at the vitreo-retinal surface, the NCSU team has proceeded to design and construct the components of the prosthesis system to be utilized in animals testing and ultimately for chronic implants in humans. A block diagram which represents the prosthesis system considered for human use is provided in Figure 1.1. The vertical dotted lines emphasize the dual unit nature of these design, with the extraocular unit consisting of the components to the left and the implantable portion shown to the right. This thesis describes the implementation of the sections in this prototype design.



Figure 1.1: Proposed system diagram for the retinal prosthesis prototype

1.3.1 Extraocular unit

The extraocular unit consists of the components which are not implanted inside the eye. These include the system image processor and the primary side telemetry unit for wireless transmission of power and instruction data.

1.3.1.1 FPGA controller

The central master controller of the prosthesis, discussed in Chapter 2, resides external to the eye in keeping with the desire to facilitate easy upgrades in future revisions. This consists of a hardware-reconfigurable image processor based on FPGA technology which functions to produce real-time instructions for the implantable stimulator IC. These instructions are based on video data from a CMOS mini-camera or derived from parameters specified manually from a laptop PC, linked to the extraocular unit with either a RS232 cable or wirelessly with RF transceivers. The extraocular unit has also been adapted for use in animal experiments, as discussed in Chapter 2. The FPGA-based image processor ultimately produces a *clock* and serial digital *data* stream for the stimulator IC.

1.3.1.2 Primary side telemetry

The next four blocks indicated as the *PWM encoder*, *ASK modulator*, *class-E power amplifier*, *power recovery*, and *clock and data recovery* as well as the extraocular coil represent the primary side telemetry system. This arrangement in Figure 1.1 indicates the topology adopted for the first generation prototype system.

Previously, invasive tethering to implanted electronics using percutaneous connectors has been used to facilitate the studies of long-term bio-compatibility and the investigation of the necessary signal pre-processing needed to enhance the performance of implants [62], [63]. However, in all cases of chronic prostheses, but especially with the ocular prostheses (owing to the eye's fragility), percutaneous connectors are unsuitable. Therefore, the common types of non-invasive connections to bio-implants and the current progress of bio-telemetry are summarized as it relates to the power and communication needs of prostheses.

The use of transcutaneous, or wireless, connections is justified due to the following

complications which are typical for alternative schemes:

1. risk of infection

Percutaneous connectors (physically wired links between implanted and exterior prosthesis components) raise the risk of infections due to a perpetual breach of the body, through which wires must pass.

2. adverse reaction to excessive movement

Depending on mechanical anchoring, such as to bone, percutaneous connectors may restrict movement of a prosthesis in the tissues in which it is implanted and with which it interfaces electrically. These tissues may be free to move with respect to a percutaneous connector with obvious complications.

3. breakage of leads or device dislodging

In the case of ocular prostheses, rapid eye movement can break any penetrating wires passing through the scleral wall, for example, which might otherwise be used to connect an intraocular prosthesis to external electronics. Furthermore, dislodging of the implant due to external tethering on the wires could occur [41].

4. battery replacement

In the case of most all prostheses, implantable batteries are undesirable because of the associated replacement surgery (except where charging can be initiated from outside of the body, as from coils, for example). Even renewable cells have limited recharge cycles. Furthermore, as a consequence of the biological environment, implanted batteries must be enclosed in the implant encapsulant, which would complicate replacement.

A wireless link must provide adequate power to an implanted prosthesis. Devices functioning as stimulators also require configuration and stimulus data to function. Furthermore, in the case that the implant also performs neuro-recording and/or monitors bio-functions, device status, or performs self-diagnostics, then there is also the need to transmit data to exterior devices. This functionality is sometimes termed *back-telemetry*. Therefore, in the general case, the success of prostheses for the long term requires a telemetry link which can provide adequate power to all implanted electronics and support a means to communicate information bi-directionally. Optical and magnetic (inductive) telemetry are considered to have the potential of meeting the goals of simultaneous power and data delivery to implants, and are expounded in the following sections.

1.3.1.2.1 Optical telemetry

Optical telemetry typically appears in ocular prostheses, since the cornea and crystalline lens are usually transparent [25]–[27], [64]. This form of telemetry uses a source of high energy light, such as a laser, to excite photoelectronics which form part of the implant. The architecture of the prosthesis reported in [25] employed a photodiode array and stimulator attached to either side, respectively, of a thin-film polyimide electrode array and anchored near the vitreous base. A supply level of 300μ A at 7v was derived from exposure to a 30mW, 820nm laser. Reported inconsistent power recovery associated with problems of uniform illumination of the photodiode led to a second generation architecture with improved electronics mounted in the crystalline lens position on a polymer annulus. Stimulation data was transmitted via intensity modulation of the external laser. No back telemetry facilities appear to have been provided. A similar development is reported in [64], in which a photodiode yielding 7v at 0.7mA with 200kbits/sec of data bandwidth has been achieved. Optical telemetry has also been successfully implemented for reverse communication [65] and is deferred to the discussion of back-telemetry in Section 1.3.2.3.
1.3.1.2.2 Inductive/magnetic telemetry

Inductive telemetry has been the standard means of wireless connection to implanted devices for years [66], [67]. It is based on the mutual magnetic coupling of two proximal, co-axial, and co-planar coils. The secondary coil in this arrangement is implanted along with the stimulator/neuro-recorder which it services, while the primary coil remains exterior. A low frequency carrier (*ie*- usually 1-10Mhz) is driven onto the primary coil which can then be coupled onto the secondary coil for transfer of power. Furthermore, this power carrier can be modulated to communicate a data-stream to the implant. This arrangement forms the basis for inductive coupling, while the precise details of how the primary coil is excited and modulated and how DC power and data are recovered on the secondary (implanted) side are varied and continue as topics of research.

Two major disadvantages are noted here regarding magnetic coupling, which are simply a characteristic of the coils. These impact the development of the primary-coil excitation and modulation circuits on the exterior (non-implanted) side.

1. Direction of radiation

It is obviously desirable to radiate energy only towards the secondary coil. In reality, the primary coil radiates energy widely in many directions, particularly with no ferrous core to concentrate the magnetic flux, as in a transformer. This omni-directional radiation pattern imposes unnecessary drain of the system batteries. It also potentially imparts EMI to other nearby electrical devices, with associated FCC implications.

2. Poor coupling

Due to the implantation, the coils must be disjoint and subsequently cannot be coupled, or linked, by a common ferrous material, but are rather "air-cored". Therefore, the mutual-inductance, or coupling-coefficient, is quite low. This requires high magnetic field strength in the primary coil in order to induce sufficient energy in the secondary coil to power the implant.

Therefore, there are three criteria which are used to optimize the inductive link performance for use in bio-implants. The first is *power-transfer efficiency*. This is a measure of how well energy in the primary coil is coupled onto the secondary coil. The optimization of this parameter is emphasized here, since achieving adequate power for the implant is of first priority. The second design parameter is *driving efficiency* which is a measure of how much power from the supply rails is dissipated in the driving circuit compared with exciting the coil itself. This obviously has a direct impact on system battery life. The third issue is *carrier-modulation bandwidth*. Potentially high data rates could be required for the implant to function as intended, particularly for visual prostheses. Each of these issues is covered separately with attention given to how they have been addressed in the research literature.

1. Power-transfer efficiency

Several studies have been conducted to measure the mutual inductance between two air coupled coils. Coupling strength is dependent on coil loading, excitation frequency [68], number of turns [69], coaxial alignment, coil separation [70], coil geometry [71], and angular alignment. Most of these are subject to variation in prostheses. Typical values for coil coupling are between 0.01 and 0.1. Power transfer efficiency can be improved with an increase in the coil coupling coefficient, k [71]. The efficiency is most easily achieved when the primary and secondary coils are series or parallel resonated with a capacitance of appropriate value, $C = \frac{1}{(2\pi f)^2 L}$ [72], where L is the coil's self-inductance.

2. Driving efficiency

Modulation techniques for data delivery are typically performed using amplifier circuits chosen for their high driving efficiency. This relates to the additional power consumption associated with the driving amplifier for energizing the primary coil. Beyond improving power-transfer efficiency, a low coupling coefficient can be compensated by driving the primary coil at high magnetic field strength. In this case, it is essential for practical battery life, that the coil's driving amplifier be as efficient as possible.

Switch-mode DC-DC converters such as the buck, boost, Cuk, Sepic, etc. achieve a high efficiency by retaining power which is not used by the load during each cycle. Rather that dissipating this unused energy as heat, as in linear or shunt regulators, these switch-mode converter topologies trade the energy back and forth between electric and magnetic fields by resonating the coils. For inductive links, this also achieves a high magnetic field strength in the primary coil, while retaining the efficiency.

The circuit topology of choice for driving the resonated primary coil is the class-E type amplifier, first characterized in [73] and [74]. In these original contexts, the amplifier is shown to drive a resistive load as illustrated in Figure 1.2a. This amplifier differs from the class-A through class-D types in that the active device operates as a switch rather than as a current source. In inductive link applications, the resistive load is replaced by a coupled inductor, functioning as the implanted receiver coil, usually resonated for maximum coupling efficiency as shown in Figure 1.2b.

The class-F amplifier shown in Figure 1.3 [75] also boasts high-efficiency operation using the concept of harmonic termination to shunt frequency components which would cause high-power dissipation in the switch [76], [77]. However, it is generally more difficult to design than the class-E amplifier and requires a correctly sized transmission line, as in Figure 1.3a [75], or else a theoretically infinite number of resonated inductive elements to achieve the high-efficiency condition. In practice, this infinite



(a) as originally introduced (resistive load)

Figure 1.2: Class-E amplifier topology

set is usually truncated to the first two of three odd harmonics, as shown in Figure 1.3b [75]. Nonetheless, from the perspective of the research literature, the class-E topology remains the dominant choice in inductive link applications as it maintains high-efficiency with a single inductor, which also serves as the primary coil.



Figure 1.3: Class-F amplifier topology

The high efficiency of the class-E amplifier results from a low-power dissipation design condition which is imposed upon the NFET operating as a switch. The voltage drop across the switch is held at near zero when the switch is conducting current in the on state, assuming low on resistance which is typical. Because of capacitance C_1 ,

⁽b) for bio-implants (inductive load)

a non-zero voltage drop develops only after the switch is opened, by which time switch current has dropped to zero. Thus, the non-overlapping product of switch current and switch voltage throughout the cycle time accounts for low-power dissipation.

The operation of the amplifier is described in [78] as follows in reference to Figure 1.2. When the switch is closed, the L_2/C_2 branch supplies the current to the switch from prior stored energy with no current flow into C_1 . The switch drain is pulled down to ground during conduction. Assuming a low resistance, R_{on} , this condition would yield low voltage drop for the switch. As the switch is opened, the L_2/C_2 cannot instantly compensate. Therefore current must continue flowing and is now routed into C_1 , causing a rise in switch voltage through the charging of C_1 . After the current from L_2 decreases to zero, C_1 begins to supply current back into L_2 until the charged on C_1 is depleted. The switch is then closed and the cycle repeats.

A unique frequency at which the non-overlapping switch current and switch voltage condition is optimized. This frequency lies halfway between the series resonant frequency of L_2/C_2 and the parallel resonant frequency of the C_1, C_2, L_2 load network. A procedure is described in [78] to calculate the component values for a desired operating frequency, supply voltage, coil current, and other parameters, based upon an assumption that L_2 has high $Q = \frac{\omega L}{R}$, implying low resistive losses. This is most easily achieved experimentally with a woven braid of wire termed $Litz^1$ which exhibits lower resistive losses by reducing the skin-effect.

Because of the low coupling coefficient, it is expected that minor shifts in the load impedance on the secondary side will be negligibly reflected to the primary

¹The term "Litz wire" is derived from the German word "litzendraht" meaning braided or woven wire. It is constructed of individually insulated magnet wires either twisted or braided into a uniform pattern [79]. This lowers ESR by distributing the skin effect of current flow at RF frequencies across many conductors instead of one. The net effect is as if current were approximately distributed uniformly across the equivalent surface area of a single conductor.

side and thus will not affect class-E performance significantly. However, close proximity of the primary coil to metallic objects or deformations in coil geometry can alter self-inductance and equivalent resistance and may heavily disrupt proper class-E operation. Therefore, auto-compensation of the class-E frequency to changes in component values (particularly shifts in L_2) using a feedback controller maintains high operating performance [78]. The technique for this involves tapping the magnetic field of L_2 with a toroidal sensing coil in order to monitor the zero-crossing of the inductor current. A controller produces the gate drive for the amplifier switch which is synchronized with the negative-going zero-crossing of L_2 's current [78].

3. Carrier-modulation bandwidth

Many micro-stimulator designs documented recently in the literature have stimulus instructions encoded into packets for transmission using digital communication protocols [32], [80]–[83]. As mentioned earlier, it is typical for advanced signal processing hardware to remain outside of the body with only the stimulus unit and associated hardware implanted. Therefore, once a link design has been established which can support the power demands of the implant, capabilities for transmitting the data stream must be added. This is commonly accomplished by modulating the power carrier using a conventional scheme, such as amplitude, frequency, or phase shift keying, with ASK appearing as the popular modulation scheme for inductive links, as discussed below.

An amplifier is developed as shown in Figure 1.4 [84] in which the voltage developed across inductor L_2 , acting as the primary coil, is linearly related to the class-E amplifier supply voltage, V_{dd} . This result is used to perform ASK modulation of the power carrier by switching the supply voltage between two levels. Capacitor C_r is used to filter switching noise from the amplifier supply. This technique achieves a data bandwidth of 80kHz.



Figure 1.4: Supply level switching in a class-E amplifier to produce ASK modulation of the power carrier

In [78], a method is described for amplitude modulating the power carrier radiated from inductor L_2 in the class-E amplifier of Figure 1.2b. By introducing a slight duty cycle shift into the feedback controller which produces the gate drive for the switching FET, the class-E amplifier is moved slightly off of the optimum operating frequency. Reported changes of 0.1% in oscillation frequency can produce upwards of 10% decrease in primary coil current [78]. This provides a mechanism for encoding digital data onto the power carrier through amplitude shift keying of the coil current and the associated magnetic field strength. A disadvantage to power carrier modulation in resonated, high-Q circuits such as the class-E amplifier described in [78] is that forced deviations in operating frequency do not track quickly. It is evident from [78] that 5-10 cycles at best (for 760kHz operation) are required for the carrier to settle to a new steady state amplitude. This imposes constraints on achievable data bandwidth.

A further negative impact of the ASK modulation described in [78] is that in pushing the amplifier away from the "class-E" frequency, the amplifier no longer operates at optimum power, An improvement was later introduced which maintains operation at optimum frequency while also increasing achievable modulation bandwidth. This led to a U.S. Patent in 1997 [85]. It became clear that as circuit energy is traded between the magnetic field of inductor L_2 and the electric field of capacitor C_2 that the system is analogous to a swinging pendulum where energy is converting between kinetic (during motion) and potential (at the peaks of oscillation). Given this analogy, one can consider halting the oscillation with little loss of energy by suspending the pendulum at the peak of the swing. In terms of the amplifier operation, this is analogous to opening the L_2/C_2 branch at the time when all of the energy resides in the electric field. Attempting to halt circuit operation at any other time results in energy dissipation, just as if one tries to stop a swinging pendulum while it is in motion. This provides a means of performing on-off shift keying (OOSK) with greater achievable bandwidth than with the ASK modulation technique described in [78]. This became known as Suspended Carrier Modulation [85], due to the indefinitely suspendable condition of the circuit oscillation (subject to leakage). The notable disadvantage of this scheme is that the implant is not externally powered during carrier suspension and must draw power from its internal supply capacitance since the primary coil carries no current during these times.

A technique is reported in [86] for performing enhanced bandwidth ASK modulation of power carriers in high-Q amplifiers which boasts the potential for the transmission of two bits per cycle of the power carrier. This is termed *HCASK: Half Cycle Amplitude Shift Keying* and is illustrated in Figure 1.5.

In [86], the driving circuit was a class-D amplifier. For comparison with *Suspended Carrier Modulation* [85], Figure 1.5 shows a modified form of *HCASK* for use with the



Figure 1.5: Class-E implementation of the HCASK modulation technique

class-E amplifier. The primary coil is tapped at a position of approximately 90% of its self-inductance value, corresponding to 90% of its turns count. The remaining 10% is duplicated. The premise of operation is that the 90% section couples to the secondary coil as does the original 10% section on the right, referring to Figure 1.5. However, the duplicated 10% section to the left is placed at a greater distance from the secondary coil, such that it's coupling coefficient is proportionately less. Each of the two 10% inductive sections are complementarily connected to and disconnected from the circuit using bilateral switches referenced to ground. Therefore, by switching between these two sections at times when the inductor current is zero, the magnetic field coupled to the secondary coil is amplitude modulated, while the impedance seen from the driving amplifier appears to remain unchanged. This does not disturb the resonant state and gives rise to enhanced modulation bandwidth over a conventionally switched resonant L-C circuit. The bandwidth in traditional inductive link designs is reported in [85] to requite about "Q" cycles of the power carrier to complete a bit transition to within 5% of the final amplitude level (for ASK modulation), where "Q" is the quality factor of the primary coil inductor. In contrast to this, HCASK is proposed to offer a bit transition every half-cycle of the power carrier. As with *Suspended Carrier Modulation* [85], the switching of the L_2 inductance is synchronized with the carrier frequency such that transitions occur when the energy of the L-C branch resides fully in the electric field, at which times the inductor current is zero.

1.3.1.2.3 Primary side data encoding

With a realizable carrier modulation scheme in place which can coexist with the power transfer to the implant, the issue remains of encoding data for transmission. Microstimulator ICs appearing in the research literature do not possess an onboard timing reference. Therefore, the asynchronous transmission of data streams is not feasible as in established schemes such as RS232, RS488, etc. The data streams are typically synchronized to an external clock which must also be supplied to the implant. This section summarizes the mechanisms used to transmit a data stream and it's clock to the implant.

Quadrature modulation schemes afford the possibility of modulating two separate carriers with the clock and data signals, respectively. However, this is unattractive since the power carrier may be the only sinusoidal waveform available. Therefore, an alternative approach is to encode the clock and data into a new digital signal, which is subsequently used to modulate the carrier. A well-known scheme for performing this is the *Manchester* encoding algorithm. Another possible approach is to encode the clock and data into a common signal through the pulse width modulation of a digital square signal according to the data. This is used in [32], [83], and [87] where the carrier is amplitude modulated with short and long pulses to encode logic-0 and logic-1 data. In this context, pulse width modulation is used to perform this encoding such that the *clock* is manifested in the rising edges of the encoded signal while *data* is coded into the pulse widths of the signal, as shown conceptually in Figure 1.6. Logically low data is represented with pulse widths which are 50% of the clock period. Logically high data is represented with pulse widths of either 25% or 75% of the clock period.



Figure 1.6: Conceptual clock/data encoding using pulse width modulation

Since the DC-supply for the implantable stimulator IC is derived from the power carrier which is modulated with the run-time data, alternating pulse widths of 25% and 75% for logically high data are chosen to render the DC level of the power carrier independent of data content, thereby assisting to stabilize the derived V_{dd} and V_{ss} supply rails for the stimulator IC [32], [83]. Although the frequency of the power carrier is fixed while the amplitude is modulated, the exact frequency is subject to variation depending on minor geometric distortion of the coil(s), proximity to metallic objects [78], and variation in exact values of the circuit elements in the amplifier driving the primary coil.

1.3.2 Intraocular unit

The intraocular unit consists of the components which are implanted inside the eye. These include the receiving coil and telemetry circuits on the secondary side and the stimulator IC which provides the electrical excitation to the retina. Telemetry in the intraocular portion is accommodated in the blocks of Figure 1.1 labeled power recovery and clock and data recovery.

1.3.2.1 Power recovery

DC power on the receiver, or implanted, side is usually recovered in conventional ways using one or more rectifying diodes. Secondary coils are either series or parallel resonated to maximize power-transfer efficiency from primary to secondary. Power recovery schemes are designed according to the need for single or dual supply rails in the stimulator IC as it relates to whether the bipolar or monopolar mode of stimulation is used.

Biphasic stimulation capability is always designed into micro-stimulators so that the exposed metals of implanted electrode arrays are not subjected to net DC potentials. Otherwise, electro-chemical processes occurring in the biological saline, or electrolytic, environment could corrode the electrodes and/or dielectric breakdown in the electrodes could occur. Output drivers of the H-bridge type, as illustrated in Figure 1.7a, for which the tissue impedance is represented as a resistance, only work well when using bipolar electrodes. Although this can be accomplished with a single supply rail, V_{dd} relative to Gnd, two electrode contacts (output and independent return) are required per stimulus output. Monopolar electrodes (shared return) on the other hand, are better suited for use with a positive V_{dd} rail and negative V_{ss} rail relative to Gnd to actively source and sink stimulus currents to the load, as shown in Figure 1.7b. Alternatively, a second voltage rail mid-way between V_{dd} and Gnd can be synthesized on-chip for use as the shared return potential, but this approach does not appear to be implemented in the research literature.



Figure 1.7: Stimulus circuits architecture types for the bipolar and monopolar electrode configurations

Another concern with inductive link designs is that coil coupling can exceed expectations and result in recovered V_{dd} and V_{ss} levels which are dangerously high for integrated electronics in the implant. There are three potential solutions to this problem. The first and less often attempted approach is to monitor the supply levels and to detune the resonance of the secondary coil to lower the coupling coefficient and power-transfer efficiency. A second approach is to instruct the exterior electronics on the primary side via back-telemetry to lower the power transfer. A third solution is an on-chip supply regulator.

Chapter 1. Introduction

In [88] and [89], a parallel resonated secondary coil drives a half-wave rectifier. This is used with a reversed Zener diode regulator to recover V_{dd} and Gnd for Hbridge stimulus circuits. The use of bridge rectifiers with Zener diode regulators is reported in [90], [91], and [92], and is improved upon in [84] where they are used to bias a NPN BJT in series with the supply path as shown in Figure 1.8.



Figure 1.8: Zener-based regulator in the *FINESS* stimulator (*Fully Integrated Neuromuscular Electrical Stimulation System*)

Conventional PN diodes used as rectifiers can account for losses and heating because of the sustained 0.7v drop during conduction. Schottky diodes can be used to further reduce this as they offer a lower voltage drop during conduction (typically 0.5v), but are not as easily integrated with stimulus circuits since they are not usually available in standard CMOS processes. A further rectification strategy used with implantable devices is the synchronous rectifier constructed from MOSFETs [93]. These emulate the rectifying function of diodes by switching on and off accordingly with gate control automatically derived from the received carrier. With voltage drops as low as 0.1v, the synchronous rectifiers can offer heat reduction by as much as 50% [93].

1.3.2.2 Clock and data recovery

The approach taken in [83] to recover clock and data waveforms from the inductively coupled carrier on the secondary side consists of an ASK demodulator and a delay-locked loop (DLL) connected in a two-stage cascade. The demodulator circuit, shown in Figure 1.9 [83], recovers a digital signal from the data embedded in the carrier envelope.



Figure 1.9: ASK demodulator used in *Retina-3* for digital PWM extraction from the carrier envelope

The demodulator does this by producing a long term average of the carrier envelope, or threshold (indicated by the dotted line in the inset of Figure 1.9 [83] and node "B" in the circuit) which is then compared against the envelope itself (represented by the signal with 1v swing in the inset of Figure 1.9 and node "A" in the circuit). This comparison is performed with the NMOS differential pair loaded with PMOS current mirrors which are cross-coupled to provide hysteresis for noise immunity. The common source amplifier level shifts the carrier envelope to the input range of the differential pair. The comparison threshold is derived from the level-shifted envelope, using a low-pass filter formed from the PMOS device at node "B" and the capacitor at node "B". The subsequent source follower and inverter amplify the differential pair output and perform a conversion to the digital domain. This final digital output represents the encoded clock/data waveform which was produced initially on the primary side to module the power carrier.

The DLL recovers NRZ (non-return to zero) data from this signal. The clock is manifested in the rising edges of the PWM waveform and can therefore be used directly to clock synchronous logic. The data is manifested in the pulse widths of the PWM waveform. The DLL, which analyzes the pulse widths to recover the data, contains a voltage-controlled delay line (VCDL) [32] as shown in Figure 1.10 [83].

Using the phase/frequency detector, charge pump, and loop filter, the DLL attempts to match the delay of this line to the period of the PWM waveform from the demodulator, which is fixed by the primary side encoder but not necessarily predefined. Once the period is matched, the width of a pulse can be evaluated from tap #15 and tap #21 of the VCDL. The data can be directly recovered as a logical function of the delay line taps. As shown in the inset of Figure 1.10 [83], a pulse which is injected into the period-locked VCDL will conditionally assert tap #15 and tap #21 depending on the pulse duty cycle. The state of the taps will be latched by the rising edge of the following pulse entering the DLL. A pulse width of 25% duty cycle or less which is injected into the VCDL will assert neither tap #15 nor tap #21. Both will remain low. A pulse width of 75% duty cycle or greater will assert both tap #15 and tap #21 high when passed into the VCDL. However, a pulse width of nominally 50% duty cycle inserted into the line will assert tap #21 but not tap #15. Therefore, an XNOR gate will correctly produce logic-0 data for pulses of nominally 50% duty cycle



Figure 1.10: Delay locked loop in the *Retina-3* stimulator IC used for clock/data recovery

and logic-1 data for pulses of nominally $\leq 25\%$ or $\geq 75\%$ duty cycle. The state of the XNOR gate is latched at the rising edge of the subsequent pulse entering the VCDL. Therefore, these two pipeline stage delays account for two cycles of latency between a correctly aligned pulse in the VCDL and its logical evaluation at the data output.

1.3.2.3 Back telemetry

Although not implemented in the block diagram of Figure 1.1, back telemetry is a relevant topic in secondary side telemetry and is briefly discussed here. Back or reverse telemetry refers to the capability of a prosthesis to transmit information from implanted electronics to exterior, non-implanted processing devices. This is commonly implemented in one of three ways. In active telemetry, coil-based inductive links can again be used. If sufficient transparency allows, as in ocular prostheses, optical telemetry can be used. As an alternative to active methods, passive telemetry can be used.

In [92], the use of inductive coupling for back telemetry is reported. It is not desireable to have multiple discrete coils on the secondary side (for inductive reception and transmission), since this enlarges the implant and complicates encapsulation and hermetic sealing. One of the advantages of using inductive coupling in back telemetry is that the strong magnetic field needed for adequate power transfer in forward telemetry is unnecessary for transmitting data back to the primary side electronics. Since only a data signal must be transmitted in back-telemetry, the requirement of a highly efficient driving amplifier in the transmitter circuit is not as stringent as in forward telemetry where the class-E amplifier is typically used. Only sufficient energy to transmit a data signal is necessary on the implant side.



Figure 1.11: Amplifier used to back-telemeter data from the FINESS implant

An amplifier topology is reported in [92] in which a capacitance C_{set} determines the oscillation frequency, as shown in Figure 1.11. Capacitor C_t provides parallel resonance to inductor L_t at the frequency of oscillation. The coil is integrated with active electronics on-chip as a spiral inductor implemented on one of the metal layers. Although the Q factor for on-chip coils is quite low, owing primarily to capacitive coupling to the substrate, the low performance requirement for back-telemetry makes this implementation feasible. Again, this is justified when considering the hermetic packaging complications of a discrete alternative. In [92], forward telemetry is modulated at 1.8MHz, while back telemetry operates at 30MHz.

Although not emphasized greatly in the research literature, optical communication can also be used for back telemetry, as an alternative to inductive schemes. In [65], a method of optical telemetry through opaque tissue, such as the skin, is described. An implanted laser diode operating at 190mW and 22% efficiency is described. Since this represents significant power consumption on the implant side, the authors also report using an LED instead of the laser diode, in which case power consumption is reduced to 100mW, at the cost of increased light scatter.

Where inductive coupling is used for forward telemetry, passive back-telemetry on the implant side can be performed over the same set of primary and secondary coils. This almost always takes advantage of the principle of impedance reflection to the primary side. By virtue of coupling, the secondary coil's impedance is manifested in the primary coil's impedance through mutual inductance and is related by $V_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$ [94], referring to Figure 1.12.



Figure 1.12: Conventions of mutual inductance

In [95], this concept is used to communicate the value of an implanted capacitive pressure sensor which in turn resonates an implanted coil. As the capacitance is modulated by intraocular pressure variation, the impact on resonance is coupled back onto the exterior coil through impedance reflection. This is formulated more generally in [96] where it is termed *Load Shift Keying*. An NMOS FET is used to alter the secondary side circuit structure which is reflected back to the primary coil as an impedance shift. The downside of this type of impedance reflection is its potential impact on the power transfer efficiency from the external unit to the implant. Interference with power delivery and data telemetry could occur, where the class-E amplifier performance is already known to be sensitive to influences upon the primary coil's impedance [78].

1.3.2.4 Implantable retinal stimulator

Within the intraocular unit, the primary component is the integrated stimulator microchip which produces excitation currents for retinal tissue. Several neuro-stimulator devices have been designed and fabricated for electrical stimulation of tissues. In [80], the development of a stimulator is reported which accompanies a penetrating electrode array [57], [58] for eliciting visual sensations through cortical stimulation. The stimulator architecture services eight electrodes per DAC to reduce chip area and communication bandwidth. A number of stimulation devices have also been developed have penetrating electrodes co-integrated with the stimulator electronics on a common substrate [81], [82], [97]. Here again, the DACs are demultiplexed onto groups of eight electrodes intended for cortical stimulation and recording. Additional efforts are also underway to develop an implantable prosthesis based on cortical stimulation [55] with significant results reported in [56]. Moreover, work is in progress among various other researcher groups towards the development of retinal prostheses [19], [20], [27]–[29], [34]–[36], [98]–[100].

Research and development efforts at NCSU have yielded several generations of stimulation ICs designed to deliver the currents for retinal stimulation in humans, as were determined by clinical studies conducted on the visually impaired with RP and AMD [17], [18]. The first design was the *Retina-1* stimulator [101], which includes on-chip photo-sensing, processing, and biphasic stimulus current generation for a 5x5 electrode array. It then became apparent that moving the photo-sensing off-chip and replacing this functionality with a discrete, extraocular CMOS mini-camera would simplify the implant, free up silicon area on the stimulator IC for further circuit level innovations, and provide greater flexibility towards upgrading and refining image processing algorithms without incurring re-entrant surgery. This gave rise to the second generation Retina-2 stimulator IC. This device was implemented in Orbit- 2μ m CMOS and provided 100 stimulus current outputs in the monopolar configuration (common return path) which were demultiplexed from a group of twenty on-chip stimulus current driver circuits. Each such driver consists of a 4-bit binary weighted current mode DAC coupled to a bridge circuit to invert the load polarity for the generation of biphasic pulses. With photosensing circuitry now off-chip, stimulus instructions are now passed to the *Retina-2* stimulator IC using a serial digital communication protocol (*clock* and *data*) conducive for future integration with a wireless inductive telemetry link. The third generation stimulator IC, designated *Retina-3* [32], [83], is a functionally equivalent layout shrink of the *Retina-2* stimulator IC from the Orbit- $2\mu m$ CMOS process to AMI-1.2 μm CMOS. The same stimulus driver architecture and communication protocol from Retina-2 were implemented in Retina-3. In further support of inductive link integration into the prosthesis, the ASK demodulator from Figure 1.9 [83] and the delay-locked loop from Figure 1.10 [83] were implemented in the *Retina-3* stimulator IC to facilitate recovery of stimulus instructions from an ASK modulated power carrier to be transmitted to the implant inductively. The

additional rectifier, filters, and regulator circuits were not implemented on-chip.

A number of improvements to the Retina-2/Retina-3 architecture have led to the design of a fourth generation IC, designated as *Retina-3.5*. These improvements include elimination of driver to output pad demultiplexing by providing a dedicated stimulus driver circuit for each stimulus channel. Although this enhances flexibility in scheduling stimulation patterns and test scenarios, it limits the number of achievable drivers within the same IC area to less than 100 when compared with the Retina-3 design. The *Retina-3.5* architecture, explained in this chapter, provides 60 drivers circuits and outputs at 4-bit current resolution. A further improvement to the *Retina*-3 design is the replacement of the bridge circuit from Figure 1.7a with the active push/pull output stage from Figure 1.7b which sources and sinks stimulation currents. This now allows different current driver circuits to be producing anodic and cathodic phases independently, which could not be properly supported using the bridge circuit in a monopolar electrode configuration. A new communication protocol with revised packet format definitions has been introduced into the Retina-3.5 series stimulator IC, appropriate to the set of sixty unmultiplexed driver circuits. The further introduction of CRC and checksum signatures and error detection circuits into the communication protocol has led to a revised stimulator IC, designated *Retina-3.55*, the architecture, design, and functionality of which is discussed in Chapter 3.

1.3.2.5 Improvements in stimulator area utilization

Although, the minimum resolution required to yield a prosthesis effective for patient mobility is as yet unknown, it is expected from recent visualization experiments [53], [102]–[104] that more then 60 outputs will be required while maintaining the current die size in keeping with the limited intraocular space available for implantation. Therefore, Chapter 4 investigates a circuit level innovation for decreasing the size of digital-to-analog converters in the retinal stimulator IC such that the number of available output channels might be increased within the same circuit area.

1.4 Implant heating

A major concern with bio-implantable electronic devices is the heat that they will generate and to what extent this will lead to elevated temperature as it spreads throughout the tissues. A heat study conducted on a live human eve must be carefully calibrated to ensure accurate empirical predictions of thermal elevation which would be consistent with the prosthesis. Furthermore, the microchip will require as yet unimplemented on-chip temperature measurement circuits and back-telemetry mechanisms to transmit this data to the extraocular unit. At the opposite extreme, a purely analytical application of the heat equation to the eye is mathematically intractable due to the very non-homogeneous ocular composition and geometry. Therefore, a new approach is developed consisting of an iterative numerical implementation of the electromagnetic and thermal physics applied to spatially discretized models of the human head and eye, including dielectric and thermal properties for the tissues. Chapter 5 reviews the derivation of the numerical methods from the analytical equations and the development of the spatially discretized head/eye model. The results of simulated power absorption in the tissues due to inductive power and data telemetry are summarized. The results of simulated thermal elevation due to this absorption and from power dissipation in the stimulator IC are also reported.

Following the discussion of this research, an overview is presented in Chapter 6 of further work and study to be undertaken on the retinal prosthesis, with attention given to improvements in the hardware and next steps to be taken with the head/eye modeling and with the heat study. Chapter 6 offers a summary and conclusion of the thesis.

Chapter 2

Design of the reconfigurable extraocular unit

2.1 Introduction

This chapter describes the implementation of the controlling hardware for the prosthesis in keeping with the system diagram of Figure 1.1. This represents the external portion of the system and supplies instructions to the retinal stimulator IC, designated *Retina-3.5*, in a remote, manual or autonomous fashion. This also serves as a text vehicle for evaluating the *Retina-3.5* and *Retina-3.55* stimulator ICs, discussed in Chapter 3. Furthermore, it is anticipated that the system will support animal experiments in which the study of electrically active implanted electrode arrays is of interest in followup to the work reported in [61]. However, by keeping in mind a versatile and flexible design which can easily adapt to encompass new functionality, the backpack unit will also support the future study of implant acceptance, and general bio-compatibility of the prosthesis materials within the biological tissues. Reliably anchoring the stimulator IC inside the eye and mechanically interfacing with the delicate retina nondestructively are the key challenges to be overcome. Additional issues include accurate modeling and simulation of thermal distribution resulting from implant heating and from the electrical field associated with applying power using a wireless inductive link. Furthermore, adequate encapsulation of the implanted materials against the corrosive exposure to body fluids is also necessary. The backpack system is anticipated to provide a vehicle for future study of these issues.

This chapter is organized into five major sections. The specifications of the backpack unit are discussed in Section 2.2 with subsequent construction of the unit discussed in Section 2.3. The testing and evaluation of the unit are discussed in Section 2.4. Future improvements are discussed in Section 2.5 and a summary is provided in Section 2.6.

2.2 Backpack specifications

The specification defined in the system the system block diagram of Figure 1.1 calls for live video input from a external CMOS mini-camera. The prosthesis would also accept synthetic image input from an external computer communicating with the system over wired RS232, or wirelessly using RF transceivers. Image processing hardware translates images into data packets conforming to the communication protocol of the stimulator IC. An inductive telemetry link provides a wireless mechanism for supplying power and communication data to the implanted stimulator.

Experimental trials in laboratory animals permit a simplified form of Figure 1.1 to be used, wherein some of the components can be omitted as shown in Figure 2.1. Synthetic images from a controlling PC are sufficient rather than live video from the camera. Furthermore, electrical stimulation of degenerate retina can be performed with an extraocular stimulator IC, pending completion of the inductive link. Therefore, these components can be omitted, such that all components except for the electrode array can be external to the eye.



Figure 2.1: Backpack retinal prosthesis block diagram for animal trials

2.3 Backpack construction

The backpack stimulator is a portable unit which can inserted into an animal vest, in this case dogs, and be configured to operate autonomously. Photos depicting the assembled backpack unit are shown in Figure 2.2 and Figure 2.3. The unit contains three interconnected boards for system power, host control, and biphasic pulse current generation for retinal stimulation based on the *Retina-3.5* stimulator IC discussed in Chapter 3. These are packaged together in an impact-resistant polycarbonate NEMA-4X enclosure.

The attachment of numerous cables to the unit is depicted in Figure 2.2 and Figure 2.3. The "RS232" connection provides a wired communications link to an external desktop PC or laptop providing commands to the unit. Power can be taken from either a battery(s), AC adaptor, or bench-top supply, with all further system voltage



(a) External view

(b) Internal layout

Figure 2.2: Right/front view of the backpack unit

levels derived internally as discussed in Section 2.3.1. The port labeled "FPGA config/camera" is a 25-pin multiplexed connection with seven of the signals allocated to backpack configuration as discussed in Section 2.3.2 and the remainder of the pins reserved for future connection with the external CMOS minicamera. The "stimulus outputs" port provides the connection point for an electrode array in the monopolar configuration which taps 25 of the available 60 stimulus circuits from the internal *Retina-3.5* stimulator IC. The "electrode ground" provide a common return path for the 25 stimulation currents. The "sync recording" output can be programmed to deliver a synchronization pulse to coordinate cortical recording equipment with the delivery of electrical stimulation from the backpack through the electrode array. A brief overview of the *Retina-3.5* stimulator IC enclosed within the backpack unit is provided in Section 2.3.3 with the detailed discussion deferred to Chapter 3.



Figure 2.3: Backpack unit with operating cables attached

2.3.1 Power supply to the backpack

The bottom board supplies DC power to the controller and stimulator IC. For efficiency, the supply is constructed from commercially available switchmode DC-DC converters, as shown in the schematic diagram of Figure 2.4. External power is supplied from a DC source in the range of 5Vdc to 12Vdc, with the current source requirement inversely related to the supply voltage (for constant power input). At 5Vdc, a 1A supply is sufficient.

Converter U₁ produces a 12Vdc supply which is reserved for future integration of the wireless inductive link to an implanted stimulator IC. It offers 1A output current with regulation efficiency up to 82%. Converter U₂ provides ± 5 Vdc with ± 1 A output current capability at up to 78% efficiency for supplying the V_{dd}/V_{ss} rails of the the *Retina-3.5* stimulator IC contained within the backpack. This will not be needed after the stimulator IC is implanted and derives its power from the wireless inductive



Figure 2.4: Backpack power-supply schematic

link. Converters U_3 and U_4 provide 5Vdc and 3.3Vdc, respectively, for the FPGAbased backpack controller and video processor. These supplies provide 1A and 3.5A output capabilities at efficiencies up 77% and 88%, respectively. Converters U_5 and U_6 provide alternate $\pm 7V$ supplies for *Retina-3.5*'s V_{dd} and V_{ss} rails in order to support higher stimulation currents [41]. These provide ± 140 mA output current capability at up to 75% efficiency. Since converters U_4 , U_5 , and U_6 have a more narrow voltage input range, they are supplied from the output of one of the previous converters. They are selectably powered from either converter U_2 or converter U_3 using jumper switches. Furthermore, all converters can be powered down if not in use, by removing jumpers from the converter inputs. A photograph of the fabricated power supply is given in Figure 2.5.

2.3.2 Backpack controller

The backpack's system controller logic is formulated in Verilog and is implemented digitally in a CPLD/FPGA device (Complex Programmable Logic Device). This permits controlling algorithms to be implemented directly in hardware, while remaining



Figure 2.5: Backpack power-supply subsystem

completely reconfigurable in support of rapid prototyping. The board associated with the FPGA is the second in the backpack unit as indicated in Figure 2.2.

A schematic of the backpack's controller is provided in Figure 2.6. The FPGA represents the hub of the design and can by virtue of its flexibility achieve any connection among of the peripheral components in support of versatile video processing and stimulator control. Since the FPGA chosen for this design has a large capacity, its configuration storage is based on SRAM (not EEPROM) and is therefore volatile. Hence, upon power-up the FPGA must be configured, or programmed, using a binary file manifesting the backpack logic design, which is compiled by a synthesizer and router from the Verilog source code. This binary file is serially clocked into the FPGA upon power-up through the use of the parallel port on the external host computer. Once the FPGA is configured from the binary file, run-time data communication with the FPGA from the external computer is currently mediated over standard 3-pin wired RS232 (transmit, receive, and ground).

In the future, the FPGA is expected to interface with an external camera as a video source for the implant, with associated image processing subroutines incorporated into the FPGA logic design. Therefore, an interface is reserved on the FPGA for image acquisition from an external digital camera. In this case, the associated pixel clock from the camera is frequency doubled by a phase locked loop and subsequently used as the FPGA clock, thus providing two cycles per pixel to facilitate image acquisition, storage, and processing. The FPGA also provides the *clock* and *data* inputs to the *Retina-3.5* stimulator IC, while it remains in the backpack. The FPGA board maintains real-time host control over the stimulator IC. Operating instructions are transferred from the external computer to the backpack, where the FPGA translates these into direct commands to the stimulator IC.

Three independent 10ns, $512\text{kB}\times8$ -bit SRAM memories acting as frame buffers, fb1-fb2, provide memory for future image processing and storage with support for dual buffered applications. A "pointer memory" implemented from three additional SRAMs connected in parallel offers a means for address translation into any one of the three frame buffers for arbitrary spatial transformation of images. Beyond this hardware architecture, the design can be refined through changes to the Verilog logic description, which in turn alters the FPGA's internal configuration definition. The internal parasitic capacitance of the FPGA's switchable interconnect structure in support of high capacity, limits the speed of practical logic designs to about 30Mhz, which is acceptable for the backpack. A photograph of the top and bottom views of the FPGA controller board in the backpack unit is given in Figure 2.7.



Figure 2.6: Schematic of the FPGA-based backpack controller



(a) top view



Imaging frame buffers RS232

(b) bottom view

Figure 2.7: Board layout of the FPGA-based backpack controller

2.3.3 Retinal stimulator IC

The *Retina-3.5* stimulator IC is intended to be an implantable device. But, in order to facilitate empirical study of the retina's tolerance to long-term electrical stimulation, while continuing to address the challenges of implant encapsulation, the micro-stimulator (shown in Figure 3.26 in bare die form) is bonded in a PGA package and placed in the backpack unit. Subsequently, retinal stimulation is performed from outside of the eye with connection to the retina conducted through the sclera. In this arrangement, the interface to the retina is achieved using a silicone-based electrode array[61] of 25 platinized stimulation sites arranged in a 5x5 matrix. This can be attached to the surface area of interest using retinal-tacks [42], [43].

The Retina-3.5 stimulator IC provides sixty biphasic pulsatile stimulation currents. The amplitudes of the anodic and cathodic phases are independently programmable for all sixty drivers with 4-bit resolution for each phase. Full-scale currents are programmable at levels of 200μ A, 400μ A, or 600μ A, subject to the extent of retinal deterioration[18], while maintaining 4-bit amplitude resolution over the selected range. Pulse timing is not independently programmable for all drivers. Pulse widths and interphase delays are configurable for each driver from a globally shared memory-bank of timing parameters. The backpack unit makes available a subset of twenty-five of the sixty drivers for animal experiments. The full set of sixty drivers are available when the Retina-3.5 stimulator IC is implanted (*ie*- used outside of the backpack unit).

Real-time programming of configuration and stimulation data for the stimulator IC is performed digitally through a serial *data* input and an associated *clock* input. On-chip data-stream synchronization is monitored and maintained to prevent erroneous communication in the event of data stream misalignment, such as a dropped bit(s), etc. Furthermore, 32-bit cyclic-redundancy and 16-bit checksum error detection mechanisms are applied to programming data to confirm intended stimulus instructions.

2.3.4 Backpack control from the external computer

The external host PC governs the activity of the stimulator IC from a software control-panel interface which runs under the Linux/X-Windows operating system. This control-panel, illustrated in Figure 2.8, provides access to the anodic and cathodic pulse amplitudes for all sixty drivers. Timing parameters for the stimulation pulses are also configurable through this software.

When controls on the panel are accessed which affect simulator specific operating parameters, special subroutines coded into the control-panel software are called which translate user commands into instructions for the FPGA. These instructions are encoded into packets for transmission from the host PC to the backpack unit, using the RS232 serial protocol at 8-bits, odd-parity, and 115.2kbps data rate. Packet formats for communication between the PC and the FPGA are shown in Figures 2.9a–2.9d for specification of driver amplitudes, timing information, full-scale current amplitude, and stimulation frame rate. When receiving an instruction packet from the host PC, the FPGA updates its own copy of the associated parameters with the new values and uses this information to synthesize instructions for transmission to the *Retina-3.5* stimulator IC. These instructions are in turn formatted in new packets according to the communication protocol for the stimulator IC.

The packets defined to communicate instructions from the FPGA to the *Retina-*3.5 stimulator IC include a configuration packet format for full-scale current and pulse timing specification and a run-time (image) data packet format for driver amplitude specification. The format of these packets is given in Figure 3.2 and Figure 3.3, respectively, and explained further in Chapter 3 in the discussion of the micro-stimulator design. Communication with the stimulator is synchronous and occurs in continuous real-time for the generation of biphasic stimulus pulse currents.



Figure 2.8: Backpack control-panel interface


(a) *Retina*-3.5 pulse profile (timing) specification packet



(b) *Retina*-3.5stimulation frame rate (clock period) specification packet



(c) Retina-3.5full-scale DAC current specification packet



(d) *Retina*-3.5 driver selection packet

Figure 2.9: Packet format definitions in the communication from the host PC to the FPGA in the backpack unit

2.4 Testing and results

The evaluation of the backpack unit in terms of its suitability as a remote, manual or autonomous controller of the *Retina-3.5* stimulator IC is discussed in Section 2.4.1. Power consumption of the FPGA controller and stimulator IC together as a unit are provided in Section 2.4.2.

2.4.1 Backpack evaluation

At this time, the backpack is configured to accept from the control panel of Figure 2.8 explicit communication of the parameters required by the *Retina-3.5* stimulator IC, including pulse amplitudes and timing in the packeted form indicated in Figure 2.9. This corresponds to the "parameterized" mode in which the backpack receives this data and reformats it into the protocol required for delivery to the stimulator IC, as indicated in the packet format definitions of Figure 3.2 and Figure 3.3. The backpack repeatedly sources to the *Retina-3.5* stimulator IC the same data packet until parameter updates are indicated from the control panel and delivered to the backpack. Any transmission from the PC to the backpack unit of updated pulse profile timing information or other parameters which are part of the configuration packet definition of Figure 3.2 will cause the backpack to send a new configuration frame to the *Retina-3.5* stimulator IC at the end of the current data frame.

The Verilog HDL description encompassing all of this controller logic is written and compiled to operate within the single chip FPGA device on the processing board of Figure 2.7. This logic design equips the backpack to receive stimulation instructions from the external computer and to generate configuration and run-time data packets for the *Retina-3.5* stimulator IC. In this way, the control panel software of Figure 2.8 yields remote and manual control of all of the design capabilities of the *Retina-3.5* stimulator IC.

Flexibility in shaping the stimulation waveform and the versatility of the system as a whole are important aspects in the prosthesis design specification. As neuroprosthetics research is a maturing field, particularly in the case of visual prostheses, a system which can easily adapt to incorporate additional capabilities is much more valuable in contrast to one exhibiting static functionality. Thus, the *Retina-3.5* stimulator IC is designed to support easy programmability of stimulus currents amplitudes, pulse widths, and repetition rates. The FPGA processing board was also constructed with such flexibility in mind. Logic synthesis results indicate that the FPGA device utilization for this application is 16% of internal memory and 33% of the onchip programmable logic cells. A much larger portion of the device resources remain available to be used whenever the backpacks capabilities must be extended beyond the current design to support additional functionality. Typical stimulus waveforms which can be obtained from the enclosed *Retina-3.5* stimulator IC inside the backpack unit are shown in Figure 3.12-Figure 3.16 with further discussion of the performance of Retina-3.5 as a stimulator IC deferred to Chapter 3. The physical size of the unit including connectors is $7.5^{\circ}L \times 3.25^{\circ}W \times 4^{\circ}H$ with a weight of 1.47 pounds, which is acceptable as a backpack stimulator for use with animal experiments.

2.4.2 Power consumption

The power consumption of the backpack unit and the internal, packaged *Retina-3.5* stimulator IC was experimentally measured collectively as a single unit, with results summarized in Table 2.1. Since power consumption is dependent on stimulator IC operation conditions and the exact shape of the stimulus waveform in particular, a number of scenarios are considered. The first case considered holds the *Retina-3.5* stimulator IC in an idle mode. Although the IC is powered at $V_{dd}/V_{ss}=\pm5$ Vdc, the FPGA is programmed to suspend the *Retina-3.5* clock and data stream.

V_{dd} ,		frame	pulse	power at				
V_{ss}^{1}	$current^2$	rate ³	$width^4$	$V_{batt} = 4V$	$V_{batt}=5V$	$V_{batt}=6V$	$V_{batt} = 7.2 V$	$V_{batt} = 12V$
	А	$f = \frac{1}{T}$	W	$P_{backpack}^{(25)}$	$P_{backpack}^{(25)}$	$P_{backpack}^{(25)}$	$P_{backpack}^{(25)}$	$P_{backpack}^{(25)}$
$[V_{DC}]$	$[\mu A]$	[Hz]	[ms]	[mW]	[mW]	[mW]	[mW]	[mW]
+5, -5	0	0	0	687.6	692.0	691.2	699.1	769.2
+5, -5	400	50	1	718.8	707.0	706.8	709.2	780.0
+5, -5	400	50	2	736.4	720.5	718.8	724.3	794.4
+5, -5	400	50	3	750.4	733.0	730.8	735.8	805.2
+5, -5	400	60	1	723.2	708.0	706.2	713.5	783.6
+5, -5	400	60	2	740.8	723.5	721.2	727.9	796.8
+5, -5	400	60	3	758.4	739.5	736.2	742.3	811.2

Table 2.1: Experimentally measured power consumption of the backpack unit

¹Due to a shortcoming in *Retina-3.5* operation at $V_{dd}/V_{ss}=\pm7V$ (see the anodic and cathodic current mismatch of Figure 3.18), the experimentally measured power consumption and dissipation for validation with the results of Table 3.2 were conducted only for the cases of $V_{dd}/V_{ss}=\pm5V$.

²Anodic and cathodic pulse amplitudes measured experimentally at $V_{dd}/V_{ss} = \pm 5$ V were 400 μ A and -408 μ A, respectively.

³Because stimulus timing is derived from a 12MHz master clock on the extraocular FPGA processor, actual frame rates are 49.827Hz and 60.048Hz, rather that 50Hz and 60Hz, respectively.

⁴Because stimulus timing is derived from a 12MHz master clock on the extraocular FPGA processor, actual pulse widths are 1.023ms, 2.046ms, and 2.991ms at 50Hz stimulation and 1.045ms, 2.025ms, and 3.004ms at 60Hz stimulation, rather than 1ms, 2ms, and 3ms, respectively.

The parameter, V_{batt} , corresponds to the single backpack power supply rail, which would be derived from a battery(s) in practice. The DC-DC power converters on the supply board of Figure 2.5 are rated to accept an input voltage on V_{batt} in the range of 3.5v to 16v. Therefore, the measurement data in Table 2.1 considers several values of V_{batt} , namely 4V, 5V, 6V, 7.2V, and 12V. The input current I_{batt} varies inversely with V_{batt} such that the input power $P_{backpack}^{(25)}$ ¹ remains approximately constant. The trend of lowest power seems to occur for V_{batt} =6V, for which the worst case power consumption associated with 400 μ A, 60Hz, 3ms biphasic stimulus currents corresponds to 736.2mW. This is associated with a worst case measured input current of I_{batt} =122.7mA. Accordingly, a 6V sealed lead acid battery of dimensions 2.76" ×1.85" ×4.25" has been located weighing approximately 1.98 pounds.

 $^{^1\}mathrm{Assumes}$ that only the 25 drivers tapped from the set of 60 available drivers in the Retina-3.5 stimulator IC are simultaneously active

This weight is comparable to that of the backpack unit such that the backpack can be loaded into the side pouch of a zip-in vest worn by a laboratory animal while the battery occupies a zip-in pouch on the opposite side, thereby maintaining a balanced load. This battery offers a rated capacity of 4.0A-h which would operate the backpack unit for approximately 32.6 hours at $I_{batt}=122.7$ mA.

2.5 Design enhancements

The backpack architecture diagram of Figure 2.1 suggests the inclusion of an RFlink to the backpack, which at this time has not yet been integrated. Currently, a three-conductor (transmit, receive, and ground) RS232 serial cable is used to provide a direct connection to the external computer running the control software of Figure 2.8. To build upon the current foundation, the introduction of wireless RF communication modules between the laptop and the backpack is considered in order to impart greater mobility to an animal wearing this unit.

Since the *Retina-3.5* stimulator IC is contained within the backpack unit as indicated in Figure 2.1, such that only the thin-film, or silicone-platinum electrode array enters the biological tissue, power converters have been included on the supply board of Figure 2.5 in support of the embedded stimulator IC. These would be unnecessary after the future integration of the wireless inductive power and data telemetry link. In this case, the connection of the exterior transmitter coil to the unit would replace the 25-conductor electrode connector. Accordingly, the *Retina-3.5* stimulator IC would be removed from the enclosure and would be designated as an implantable component consistent with the block diagram of Figure 1.1.

The "parameterized" mode discussed in Section 2.4 is currently the only mode developed to run of the adaptable backpack hardware. The expanded mode to be implemented in the future is the imaging mode, whereby the control panel will send a pixelated image to the backpack unit, to be internally processed and converted into a serial, digital data stream for the stimulator IC. This image can be of the same spatial resolution as the number of current driver circuits, or output channels, or can be of higher resolution such as a 320×240 image from the video camera. In the latter case, the FPGA in the backpack would perform further spatial processing involving pixel neighborhood computations, etc. in order to efficiently condense the additional pixel information down to the resolution of the *Retina-3.5* stimulator IC, which is 8×8 (minus the four corners, as only sixty drivers circuits are available). In both cases, a separate 256×16 -bit conversion table could be loaded into the backpack to function as a "color palette" would in the conventional sense to translate 8-bit image pixel intensities into 16-bit driver data subpackets, formatted as shown in Figure 3.4. This provides a well defined and programmable mechanism to render image information into the pulse amplitudes and timing data necessary for the *Retina-3.5* stimulator IC. The mode described here is best understood as the "still imaging" mode, in which real or synthetic test images can be loaded into the backpack to be repeatedly presented to the stimulator IC at any programmable stimulation frame rate (upwards of 300 frames/second). Realistic frame rates for retinal stimulation are closer to 60Hz which would be above the flicker fusion rate of 40Hz reported in [18]. This would support experiments to assess the quality of vision from the retinal prosthesis. Each of the three $512kB \times 8$ -bit frame buffers would support six 320×240 resolution images loaded simultaneously for a total of 18. A natural extension to the still imaging mode is the video imaging mode in which an external CMOS video camera supplies input formerly

provided by the external computer. In the video mode, the FPGA could continue to perform the same image processing on behalf of the implanted stimulator IC. These operating modes are summarized in Table 2.2.

Mode	Description	Status
parameterized	• data is supplied from the external computer	completely
mode	• pulse amplitude specified explicitly per driver	implemented
	• global pulse timing specified explicitly	and verified
	• full-scale stimulation current specified explicitly	
	• frame rate programmable	
	• no pixelated imaging features	
still image mode	• image data is supplied from the external computer	incomplete
	• image could be of variable resolution	(future
	• low resolution images need no spatial processing	enhancement)
	• high resolution images should be processed to use image	
	data efficiently	
	• translation table supports conversion of image pixel	
	intensities into driver data subpackets	
live video mode	• video data is supplied from the external camera	incomplete
	• images should be processed to use image data efficiently	(future
	• translation table supports conversion of image pixel	enhancement)
	intensities into driver data subpackets	,
	• fully automated: required no on-going input from the	
	external computer	
	-	

Table 2.2: Present and future operating modes for the *Retina-3.5* backpack unit

2.6 Summary

A backpack unit is presented as a portable stimulator for evaluating retinal prostheses in animals. The unit can be interfaced to an external computer for configuration, control, and monitoring. Once programmed with stimulation instructions, the unit is autonomous and can be detached. Hardware support for image acquisition and processing is included in the backpack unit for future connection to an external camera. A PGA-packaged sixty-channel micro-stimulator IC, *Retina-3.5*, is included in the backpack for extraocular electrical stimulation of the retina through a twenty-five site electrode array. Complete control of the stimulator can be maintained from the external computer. In future experiments, where the stimulator IC is implanted, the backpack unit can again be used to control the stimulator by expanding it with a wireless inductive link for power and data telemetry.

Chapter 3

Design of the intraocular retinal micro-stimulator

3.1 Introduction

Our current retinal prosthesis prototype system consists of an extraocular unit including image acquisition and processing, telemetry encoder, power amplifier, and transmitter coil, as shown in Figure 1.1. The intraocular unit consists of a receiver coil, power recovery in the form of a rectifier and regulator, clock/data recovery, and the retinal stimulator. This chapter focuses on the retinal stimulator block of the prosthesis system diagram, and in particular improvements to the *Retina-3* and *Retina-3.5* IC designs.

This chapter is organized into three major sections. The architecture, functionality, and circuit design of the stimulator IC are described in Section 3.2. An overview of measurement results is given in Section 3.3. A discussion of scalability and improvements to the design is offered in Section 3.4 with a summary given in Section 3.5.

3.2 Retina-3.5/Retina-3.55 stimulator IC design

The *Retina-3.55* stimulator IC described here is functionally identical to the *Retina-3.5* but with revised, more robust synchronization monitoring in the packet parser controller and the addition of CRC and checksum signature generation and error

detection subcircuits which assist to validate the input data stream. Functional specifications for operation as an implantable stimulation device for a retinal prosthesis call for excitation currents up to 600μ A amplitude [41] delivered to retinal tissue with characterized impedance of approximately $10k\Omega$ [61]. Variable stimulation rates of 50-60Hz and up are desired to achieve flicker fusion as well as definable pulse widths and interphase delays on the order of 1-5ms [18]. Simulation pulses are produced in the standard biphasic fashion with anodic-leading or cathodic-leading charge-balanced pulses for compatibility in the biological environment. The device is designed to provide sixty excitation channels with reference to a common return potential (monopolar electrode configuration). To achieve greater flexibility over the *Retina-3* design in programmable and connect directly with sixty output channels (or pads) with no demultiplexing circuits. This provides a single stimulation frame, and thus an intended visual experience in the form of an 8x8 pixelated image (minus the four corners).

A block diagram of the architecture of the *Retina-3.55* stimulator IC highlighting the major circuits structures and connectivity is depicted in Figure 3.1. The IC interfaces with the external world through six pins: three power rails, V_{dd} , V_{ss} , and Gnd, and three control signals, which include an active-low *reset*, a rising-edge triggered *clock*, and a serial digital *data* input. Sixty additional output pads are reserved on the I/O pad ring for the stimulus current channels.

As with the *Retina-3* IC, two types of formatted data packets for *configuration* and *run* (imaging) data are defined for the *Retina-3.55* IC and are discussed in Section 3.2.1. Synchronization detection and maintainance with the externally supplied data stream is explained in Section 3.2.2, while protection against errors in this data is described in Section 3.2.3. Timing control of the stimulus pulses is discussed in



Figure 3.1: Block architecture of the *Retina-3.55* micro-stimulator IC

Section 3.2.4 with control of the pulse amplitudes explained in Section 3.2.5.

3.2.1 Communication protocol

The instructions which specify the operation of the stimulator are defined digitally and loaded into the IC serially through a *data* input and accompanying *clock* input. A *configuration frame* packet format is defined for specification the full-scale output current magnitude and stimulus timing, including pulse widths and interphase delay. An additional packet format, designated as the *data frame*, is defined for specifying desired stimulation current amplitudes per phase, or for requesting charge cancellation, for all driver circuits in real-time, thereby constituting a single image frame. Both of these frames are 1024 bits in length, which is convenient for delimiting frame boundaries as packets are loaded.

3.2.1.1 Configuration frame packet format

The format of the configuration-frame packet is illustrated in Figure 3.2.

1023	1008	"	177	175 168	167 16	0 159 15	52 151 14	4	"	63 56	55 48	47		16	15 0
config sync v	vord XXX ··	· "… 🕅	$I_1 I_0$						°				CRC signature		checksum
		a	176	ł	Ś	Ş			a	{	{				
config sync	word = B368 (0 uA,	(hex) if 00	maximu	profile-1	profile-1	profile-2	profile-2			profile-8	profile-8				
maximum curre	$ent = \begin{cases} 200 & 0 \\ 400 & 0 \\ 600 & 0 \end{cases}$	A, if 10 A, if 10 A, if 11	m current	start time	stop time	2 start time	2 stop time			3 start time	3 stop time				

Figure 3.2: *Retina-3.55* configuration frame packet format



Figure 3.3: Retina-3.55 run-time data (image) frame packet format

A unique 16-bit synchronization word identifies the beginning of a configuration frame. Once the sync-word is located, the stimulator IC assumes that successive data pertains to configuration. Following the synchronization word are 830 "don'tcare" bits. Following these are two bits which define the full scale amplitude for the current-mode DACs in the output drivers. Full scale currents are globally selectable (for all drivers) as 200μ A, 400μ A, or 600μ A, with the full DAC resolution spread uniformly across the selected range.

Following the full-scale current specification, is data which defines the start and

stop times for eight independent global on-chip pulse profile subcircuits, which establish timing for the biphasic output currents produced by the sixty drivers. Each start time and stop time specification is an 8-bit number representing a count of clockcycles in multiples of four relative to the onset, or internal latching, of the frame, which is 1024 clock cycles in length.

The configuration packet format ends with embedded CRC and checksum signatures which are inserted to provide some error detection for validating the packet contents. These are discussed in Section 3.2.3. Once the synchronization word for the configuration frame is located, the error detection unit is initialized and directed to compute an internal CRC and checksum signature. After the frame is completely shifted in, these computed values are compared against the signatures embedded in the packet. If the CRC and checksum signatures both match, then the configuration data is assumed to be error-free and is subsequently latched into internal registers allocated to the configuration data where they become resident and take effect. Otherwise, the data is ignored and subsequently overwritten as new packets are shifted into the IC.

3.2.1.2 Run-time data (imaging) frame packet format

The format of the data-frame is illustrated in Figure 3.3. As with the configuration packet, a data packet is initiated with a unique 16-bit synchronization word, which is distinct from the configuration sync-word. Once the sync-word is located, the stimulator IC assumes that successive data defines stimulus current amplitudes associated with image (or pixel) data for the sixty current drivers. Following the synchronization word are sixty nested driver subpackets, starting with driver-1, each of which is 16-bits in length and is formatted as shown in Figure 3.4.

The most significant bit (bit-15) is unused. The cathodic and anodic pulse profile references select one of the eight pulse timing profiles to establish the start and stop



Figure 3.4: Retina-3.55 driver subpacket format

times for the cathodic and anodic phases, respectively, of the biphasic pulse. Any pair-wise combination of the eight pulse profiles can be specified for each of the sixty drivers, but should not be programmed to the same pulse profile within a single driver, as this would instruct the IC to overlap cathodic and anodic phases in time. Although the stimulator IC does not provide hardware interlocks to prevent this programmed condition, the chip would not be damaged by the occurrence. Only the difference in the cathodic and anodic currents would flow into the load (tissue), while the remainder would by pass the output (electrode). The cathodic amplitude specifies the current level (relative to the full-scale current specified in the configuration data) to produce during the cathodic phase. Similarly, the anodic amplitude specifies the current level in effect during the anodic phase. Bit-7 of the driver subpacket format is used to control the status of the charge cancellation facility. Each driver is capable of internally shorting its output connection back to the indifference, or return, potential in order to minimize the accumulation of any DC charge on the output electrode. The buildup of such stray charge could result from process variation induced mismatch across the stimulus driver circuit with corresponding amplitude imbalances or from other sources of charge accumulation. The following constraints should apply for the *Retina-3.55* stimulator IC to produce a correct biphasic pulse:

- 1. The correct synchronization words must be used to successfully communicate configuration and run-time data packets for conveying intended stimulus instructions.
- 2. Correctly computed CRC and checksum signatures representative of the frame data should be embedded in the packets.
- 3. A non-zero full-scale current amplitude should be programmed in a configuration packet.
- 4. Start times in pulse profile definitions should be programmed to precede the corresponding stop times.
- 5. Cathodic and anodic pulse timing profile references should not be the same for any driver circuit.
- 6. The referenced cathodic and anodic pulse timing profiles should not overlap in time for any driver circuit.
- 7. The charge cancellation feature should not be used within any driver circuit during any given data frame if the specified cathodic or anodic amplitudes are nonzero.

As with the configuration packet, the data packet ends with embedded CRC and checksum signatures for error detection. Once the synchronization word for the data packet is located, the error detection unit is again initialized and directed to compute an internal CRC and checksum signature. These are compared against the signatures embedded in the packet. If both signatures match, then all sixty driver subpackets from the data packet which were shifted into the IC are assumed to be error-free and are subsequently latched into the appropriate output-driver registers. Otherwise, the data is ignored and overwritten as new packets are shifted into the IC. The latching of this data into the drivers defines the time, t_0 , against which the pulse profile start and stop times are referenced.

3.2.2 Maintaining communication synchronization

The possibility of a drop bit(s) in communication with the implant warrants monitoring data stream synchronization within the stimulator IC. In the previous generation stimulator IC design, *Retina-3.5*, this is accomplished by verifying that the synchronization word actually appears at the beginning of each frame. The 10-bit frame length counter is initialized after a packet sync-word is detected. Therefore, as it reaches its terminal count of 1024 and thereby signals the end of the packet, the sync-word for the following packet should already be shifted into the IC and be aligned in the correction position to confirm the onset of a new packet. If it does not appear on schedule, then the stimulator ceases to parse further configuration or image data, until a sync-word is re-acquired.

In the current generation IC, *Retina-3.55*, detecting a loss of synchronization is further strengthened by the packet error detection mechanism. Packets invalidated by dropped bits should with high probability provide CRC and checksum signatures which are inconsistent with the IC's internal CRC/checksum calculations.

3.2.3 Error detection subsystem

The *Retina-3.55* stimulator is anticipated to operate in the saline environment of the human eye, isolated from the prosthesis electronics exterior to the eye. Accordingly, the inductive telemetry link discussed in Chapter 1 is necessary for wireless communication with the stimulator IC, which increases the probability that errors in communication will occur in the data stream. Without a means to detect the errors, the stimulator IC will process any data it receives. This could have unintended consequences, such as generating biphasic current signals which are not properly charge-balanced. Due to the risks associated with processing erroneous data, CRC and checksum error detection mechanisms are added to the chip specifications. This is the sole distinction between the *Retina-3.55* stimulator IC design and its immediate predecessor, *Retina-3.5.*

3.2.3.1 CRC unit

A 32-bit cyclic redundancy check (CRC) computation engine is designed and implemented as a means of evaluating data integrity for configuration frames and data (image) frames. The algorithm conforms to the ITU-TSS CRC standard with the characteristic polynomial of Equation 3.1. The circuit implementation is as shown in Figure 3.5.

$$G(x) = x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1 = 0$$
(3.1)



Figure 3.5: Circuit implementation of the 32-bit CRC

3.2.3.2 Checksum unit

To increase the robustness of error detection, the CRC computation engine is accompanied by a checksum calculation. The checksum unit maintains a 16-bit sum of all bytes in the configuration frame or data frame. This includes the synchronization word, the embedded CRC signature, and all intervening packet data.

3.2.3.3 Treatment of erroneous configuration and data packets

The additional capability of packet error detection introduced into the *Retina-3.55* stimulator IC requires some revision to the packet parsing controller. Unambiguous actions must be defined which regulate well-defined chip behavior in all possible error scenarios. These must account for errors in configuration packets as well as in run-time data packets. The original controller from *Retina-3.5* is expanded to incorporate these new actions. The state machine for this new controller has six states, with a behavior summarized in the flow chart of Figure 3.6.

Some abbreviation is employed in the diagram to clarify the flow of actions. These are elaborated in Table 3.1. It is critical to understanding Figure 3.6 that the reader realize that the status signals in the controller do not all refer to a common packet. Recall, that *Retina-3.55* is designed to parse in new packets while simultaneously attending to prior packets which were latched for processing. The *CRC_matches* and *checksum_matches* flags refer to packets whose delivery to the chip is about to complete. Similarly, the *profile_inhibit* flag refers to packets which were latched for processing. In contrast, the *rsync* and *csync* flags are associated with the recognition of synchronization words in configuration frames and run-time data frames of the *next* packets which are beginning to arrive (*ie* -shift in through the data input pin).



Figure 3.6: Behavioral diagram of the packet parser controller in the *Retina-3.55* stimulator IC

Table 3.1: Description of signals/flags used in the behavioral diagram	of Figure 3.6
of the packet parser controller in the <i>Retina-3.55</i> stimulator IC	

Signal	Description
csync	Indicates that the synchronization word for a configuration packet (B368 hex) is recognized by the sync detector during this clock cycle
rsync	Indicates that the synchronization word for a runtime data packet (4C97 hex) is recognized by the sync detector during this clock cycle
CRC_matches	Indicates that during this clock cycle, the CRC unit flags a match between its internal CRC computation and the CRC signature embedded in the packet
checksum_matches	Similarly, this indicates that during this clock cycle, the checksum unit flags a match between its internal checksum computation and the checksum signature embedded in the packet
profile_inhibit	A signal from the packet parser controller which prevents the timing profile subsystem from generating the eight pulse timing profiles, which effectively inhibits output biphasic sti- mulation currents
cfifo	The data input to the fifo which shifts through the profile subsystem. Configuration data is routed to <i>cfifo</i> by the packet parser controller.
dfifo	The data input to the fifo which shifts through the driver array. Run-time data is routed to <i>dfifo</i> by the packet parser controller.
fifo_out	The single bit output of the 48-bit leading section of the data fifo, including the CRC unit and the checksum unit (for a prior packet) and the sync detector (for a subsequent packet) through which a configuration or run-time data packet ini- tially shifts before it is routed to either <i>cfifo</i> or <i>dfifo</i>
clatch	A signal from the packet parser controller which triggers the timing profile subsystem to latch new configuration data which has been shifted into it
dlatch	A signal from the packet parser controller which triggers the sixty stimulus circuits of the driver array to latch new run- time data which has been shifted into them
init_CRC	A signal from the packet parser controller which initializes the CRC unit for processing a new incoming packet
init_checksum	A signal from the packet parser controller which initializes the checksum unit for processing a new incoming packet

In the previous stimulator IC design, *Retina-3.5*, no error detection in the form of CRC and checksum is present in the communication protocol. Therefore, the mechanism employed to detect misalignment in communication consists only of a check at the end of each loaded packet that the synchronization word for the following packet has arrived on schedule and is currently recognized by the sync-word detector. Again, the frame length counter is initialized after a sync word is detected. Therefore, at the time it reaches its terminal count to signal packet completion, the sync word for the next packet should already be shifted in, thereby giving rise to an easily timed alignment check. A missing sync-word causes the chip to ignore subsequent information in the data stream. Moreover, it also suggests that an error such as misalignment might have occurred some where prior in the data stream, potentially invalidating the previous packet. Therefore, *Retina-3.5* was designed such that the necessary condition for processing a packet is that the sync-word for the next packet must arrive on schedule.

This behavior is retained in the *Retina-3.55* stimulator IC and is indicated in all states of the behavioral diagram of Figure 3.6 by a return to the initial state (A) should *csync* and *rsync* both return *FALSE* at the expected time for the appearance of a packet sync-word. Moreover, a packet must have a positive assertion on *CRC_matches* and *checksum_matches* in order for a packet to be accepted. Therefore, if packet synchronization is lost then the packet parser controller will return to its initial state (A) and enter into a "hunt" mode in order to reacquire packet synchronization.

The *Retina-3.55* stimulator IC will not process any run-time data defining stimulus amplitudes nor allow biphasic stimulation current pulses to occur until a configuration packet is first received without error and latched. Recall that in run-time data packets only anodic/cathodic pulse amplitudes and anodic/cathodic pulse timing profile references are encoded. Absolute timing is not specified. Therefore, if no configuration data has been loaded into the chip, then timing profiles will not be defined and it is therefore inappropriate for *Retina-3.55* to generate electrical stimulus. Any biphasic stimulus pulses would not necessarily be charge balanced. The packet parser controller design of Figure 3.6 enforces that valid configuration data must be in place before stimulus generation is enabled.

The *Retina-3.55* stimulator IC does not have *back-telemetry* at this time to support the communication of status or other data back to the extraocular host controller. Therefore, the external system cannot know when an error-free configuration packet has been received. The interim solution for this is for configuration packets to be retransmitted to the IC at a regular interval, regardless of whether they represent new configuration data. In this way, it is reasonable that *Retina-3.55* will eventually receive and latch an error-free configuration frame.

Pertinent to this scheme is the observation that any run-time data packet contents reference timing parameters which were transmitted in the most recent configuration packet. Therefore, if a configuration packet is received and is in error, then any subsequent run-time data packets are flagged as unusable. This is because the run-time data packet references faulty information transmitted in the most recent configuration packet which, in this scenario, was received by the chip with errors but can only assumed to be error-free from the perspective of the extraocular unit. Therefore, subsequent run-time data packets received by the chip are rejected regardless of their error condition. No further run-time data packets are accepted until a new configuration packet is received without error.

If a valid configuration packet has been latched internally, then subsequent errorfree run-time data packets will also be latched for stimulus generation. Pulse timing profiles referenced therein will make use of data from the the most recent, preceeding configuration frame to establish pulse widths and interphase delays. Any run-time data packet hereafter which is found to be erroneous will not be latched. The driverarray is prevented from generating stimulus during this frame duration. In forcing an idle time, it is not sufficient to suppress latching of erroneous run-time data packets, since the most recent data packet remains resident in the driver array and would be repeated, which may be undesirable. Instead, the action taken here is to inhibit the generation of pulse timing profiles from the profile subsystem using the *profile_inhibit* signal. This effectively disables chip-wide generation of biphasic pulse currents and electrical stimulus. Operation resumes upon acquisition of a run-time data packet which is determined to be free of errors. Similarly, any new error-free configuration packets would be accepted as well.

3.2.4 Profile generator design

The profile generators produce eight global pulses timing references which are independently programmable in a configuration packet. These exist in the form of 8-bit (*start* time, *stop* time) pairs. Each parameter represents a count of clock-cycles in multiples of four, relative to the start of each of run-time data frame (*ie-* when the corresponding data packet is latched into holding registers in the stimulus driver circuits. A diagram of the pulse profile subsystem is provided in Figure 3.7a.

A 10-bit counter used to parse the frame length is cleared to zero upon detection of a configuration sync-word or data sync-word, thereby signaling the beginning of the corresponding packet. If the sync-word of the new packet indicates a configuration frame, then 16-bit shift registers within each of the eight pulse profile generators, which are daisy-chained together, are shifted on each clock cycle as new serial data enter the IC. The counter is also incremented, accordingly. Once the frame is completely shifted in without errors, the new configuration data is latched into the 16-bit holding registers of the profile generators. In the interim, existing pulse timing specifications which are already resident in these holding registers provide timing during the concurrent synthesis of biphasic stimulus currents in the driver array. The gate level detail of each of the eight pulse timing profile generators from Figure 3.7a is given in Figure 3.7b.

The logical gating of the pulse profiles occurs as the upper 8-bits of the 10-bit frame-length counter are compared with the *start* and *stop* times stored within each pulse-profile generator. Once the *start* time is reached, the pulse profile is asserted logically *high*. As the *stop* time is reached, the pulse profile is returned logically *low*. This is performed in parallel for the eight pulse timing profile generators, as shown in Figure 3.7a.



Figure 3.7: Pulse timing profile generator subsystem

3.2.5 Stimulus current driver design

Each of the sixty current drivers is capable of producing a biphasic stimulus pulse current using information provided in a latched run-time data packet. For simple modeling, the retinal tissue is considered to be an equivalent $10k\Omega$ DC impedance [61], although the actual combined electrode-tissue impedance model is more complex [105], [106]. A conceptual model of the biphasic current driver is shown in Figure 3.8.



Figure 3.8: Conceptual switch-level model of the biphasic stimulus current driver circuit

The anodic current is sourced to the load by an ideal current source referenced to a positive supply of V_{dd} . Similarly, the cathodic current is sinked from the load by an ideal current source referenced to a negative supply of V_{ss} . The driver circuits deliver output current to monopolar electrodes which are referenced to a return potential of ground, *Gnd*. The electrode array [61] might be attached to the retina using retinal-tacks [42], [43].

Note that for an N-well process, where all NMOS FETs share a common bulk potential in the IC substrate, the V_{ss} supply imposes a constraint on the digital logic

circuitry. To minimize body effect in the *Retina-3.55* stimulator IC, all digital logic circuits and "low-voltage" analog circuits, including the DACs and most of the bias generator, operate between V_{ss} (logic "0") and *Gnd* (logic "1"). V_{dd} is used only in the output stage of the driver circuit and in part of the biasing circuit (both explained below).

The stimulus driver circuit employs two 4-bit NMOS binary-weighted currentmode DACs to produce the anodic and cathodic currents. The DAC design, shown in Figure 3.9, is designed with wide-swing cascode current mirrors referenced to V_{ss} in which the branch current subcircuits are duplicated $2\times$, $4\times$ and $8\times$ to implement the binary weighting with respect to the digital input code, D₃-D₀. The cascode NFETs, M₁-M₄, are biased directly from the signal, *dcas*, generated in the bias circuit. The current source NFETs, M₅-M₈, have their gates switchable to either *ibias*, generated in the bias circuit (yielding the ON state) or to V_{ss} (for the OFF state). This occurs under control of the digital input code, D₃-D₀. The requested current amplitude specified by D₃-D₀ is gated by the *profile* signal corresponding to an output of one of the eight pulse profile generators (Figure 3.7a and Figure 3.7b), such that the DAC current is enabled only while the profile signal is asserted logically high.

To date, the standard DAC arrangement for producing biphasic stimulus pulse currents consists of a stacked PMOS-DAC/NMOS-DAC configuration driving a monopolar electrode output [81], [82], [97]. This arrangement is conducive to stimulation when the excitation currents are small (*ie*- tens of μ A to the low hundreds of μ A). However, the electrical stimulation of RP/AMD degenerate retina appears to require currents of 0.5mA or more [41]. For a modeled load resistance of 10k Ω , currents of these magnitudes can require high supply voltages relative to normal rails in the given process (AMI-1.2 μ m for the *Retina-3.55* stimulator IC). This may require alternative transistor structures which can support high drain-source voltages without modification of



Figure 3.9: Circuit detail of the binary-weighted, wide-swing, current-mode DACs used in the stimulus current driver circuits of the *Retina-3.55* stimulator IC

the process, such as those reported in [107], [108]. Therefore, the current-driver structure is modified so that the DACs produce reduced currents at lower voltage levels, which can be mirrored and scaled into an output circuit of high-voltage compliance. The circuit for this is shown Figure 3.10, and is referred to as the biphasic amplifier. Two of the current DACs of Figure 3.9 are instantiated within the output stage of each stimulus driver circuit for implementing the anodic and cathodic current phases, respectively. The digital input codes to these DACs is taken from the *anodic pulse amplitude* and the *cathodic pulse amplitude* fields from a driver subpacket (defined in Figure 3.4), of which sixty are supplied in a latched run-time data packet.

Each stimulus current driver circuit, including the biphasic amplifier, also contains two 8-to-1 multiplexers which provide the profile inputs to the two DAC subcircuits for the anodic and cathodic current phases. These permit the programmable selection of any of the eight pulse timing profiles for establishing start and stop times for the



Figure 3.10: Circuit level detail of the biphasic amplifier output stage within each stimulus current driver circuit

anodic and cathodic pulse phases, independently. These eight signals, generated in the profile subsection of Figure 3.7a, are distributed among the driver array so as to be selectable within each driver block.

The final component of the driver circuit is a charge cancellation mechanism, which is intended to limit any unintentional accumulation of charge on the electrode, or output. This circuit functions by shorting the electrode to ground through the PFET switch, labelled M_{23} in Figure 3.10. The PFET is biased "on" via the NFET pulldown device labeled M_{22} . This is logically controlled by bit-7 of the 16-bit driver subpacket during the active time of the anodic pulse timing profile (as performed with the AND gate of Figure 3.10). The charge cancellation switch is cut-off by a passive pullup to V_{dd} using the diode connection PFET, M_{21} .

3.2.6 DAC biasing circuit

The wide-swing cascode current mirrors in the NMOS DACs and the biphasic amplifier stage receive their bias voltages from a central biasing circuit. From here, the bias voltages are distributed across the driver array. The schematic of the bias circuit is provided in Figure 3.11. The biasing circuit can be considered in three sections, which are labeled in Figure 3.11 as the *Bootstrap reference*, the *DAC biasing* section, and the *biphasic amplifier biasing* section.



Figure 3.11: Central bias circuit for the DACs and biphasic amplifiers

The *bootstrap reference* is a classical circuit which settles to the intersecting operating point of the linear I-V curve for the resistance, *rbias*, and the non-linear I-V curve for the FET transconductance of M_1 [109]. The devices are sized to achieve a $20\mu A$ master reference current, which becomes the basis for other currents produced on-chip.

The *DAC biasing* section taps the PMOS cascode current mirror in the bootstrap reference and uses this to establish the two biases, *dcas* and *ibias*, for the two NMOS anodic and cathodic DACs in the stimulus driver circuit of Figure 3.10. Using two bits from a prior latched configuration packet, (I_{ref_1}, I_{ref_0}) , the DAC biasing section can be tuned to mirror the bootstrap reference current with gains of 1X, 2X, or 3X. This scalable current is reflected into the diode-connected NMOS wide-swing cascode reference circuit in order to tuned the *ibias* potential. This allows full-scale DAC current amplitudes of 20μ A, 40μ A, or 60μ A to be achieved and ultimately permits full-scale output current amplitudes in the stimulus driver's biphasic amplifiers to be programmed at 200μ A, 400μ A, or 600μ A.

The *Biphasic amplifier biasing* section also taps the PMOS cadcode current mirror in the bootstrap reference and uses this to construct biases for the wide-swing cascode current mirrors in the output stage. The NMOS cascode bias, called *ncas*, is formed by reflecting the unscaled reference current into a diode-connected, V_{ss} -referenced NFET. Similarly, the pmos cascode bias, called *pcas*, is formed by reflecting a copy of the reference current into a diode-connected, V_{dd} -referenced PFET.

3.3 Experimental measurements

The *Retina-3.5* stimulator IC, which is the prior version of the chip described in this chapter, was implemented in AMI-1.2 μ m CMOS and occupies an area of 4.7mm×4.6mm. Since the *Retina-3.55* stimulator IC has not been successfully fabricated at this time, experimental measurements are taken from the *Retina-3.5* IC design, which contains the same stimulus driver core and is functionally equivalent to *Retina-3.55* except for

the absence of the the CRC and checksum error detection logic. The driver circuit is characterized in terms of linearity and pulse amplitude matching (Section 3.3.2), current sensitivity to power supply variations (Section 3.3.3), and effectiveness of the charge cancellation mechanism (Section 3.3.4). Power consumption requirements for the stimulator are analyzed in Section 3.3.5.

3.3.1 Output flexibility and example waveforms

A typical biphasic stimulus current pulse generated from the *Retina-3.5* stimulator IC is shown in Figure 3.12. For this figure, the chip is operated from +5v/-5v rails since the chip functions optimally at these process targeted supply levels and is driving a 10k Ω load, the nominal retinal impedance [61], referenced to ground. This is a transient plot of the voltage across the load resistance, while the stimulator IC is processing 100 frames per second.

Figures 3.13–3.14 illustrate how the anodic/cathodic pulse amplitudes can be independently specified. In order to generate a targeted current amplitude of 600μ A, the supply voltages must be increased beyond +5v/-5v (assuming a $10k\Omega$ characteristic load impedance). Although pulses are achievable at +7v/-7v, the matching between anodic and cathodic pulses degrades due to limitations in the output stage design for such high supply voltages in AMI-1.2 μ m CMOS. These supplies are beyond those rated for the process, however the gate oxides and drain/source junctions have been found to be tolerant of +7v/-7v rails without immediate permanent damage.

Figure 3.15 shows some of the variations in timing that can be achieved through manipulation of pulse timing profile definitions using a configuration packet. The drivers are programmed to deliver the maximum output current (D_3 - D_0 =1111 in Figure 3.9) at the 400 μ A full-scale current setting (Iref₁=1, Iref₀=0 in Figure 3.11).



Figure 3.12: Charge-balanced biphasic current pulse produced from the *Retina-3.5* stimulator IC (experimentally measured)

Waveform #1 is the typical case of a charge-balanced anodic-leading pulse. Waveforms #2-#4 illustrate the versatility of the chip to produce biphasic stimulus currents with independently programmable pulse widths in the anodic and cathodic phases as well as to adjust the interpulse delay, even down to zero, by carefully adjusting the pulse timing profiles using a configuration packet. Furthermore, biphasic pulses can be configured as "anodic-leading" (waveforms #1-#3) or "cathodicleading" (waveform #4). These waveforms are generated at a rate of 100 frames/second. The frame rate can be globally increased by adjusting the frequency of the chip clock input to the stimulator IC, as shown in Figure 3.16 for an increase to 300 frames/second. The maximum achievable stimulution pulse rate is 1465 pulses/sec with an associated maximum chip clock frequency of 1.5Mhz for 1024 bit packets. This is well beyond the flicker fusion rates reported in [18].



Figure 3.13: Independent amplitude variability of the anodic phase (experimentally measured)

3.3.2 Linearity and pulse amplitude matching

Figure 3.17 shows a plot of stimulation current amplitude from a single driver circuit connected to a 10k Ω load, measured as a function of the DAC digital input code (D₃-D₀ in Figure 3.9). Once again, $V_{dd}/V_{ss}=\pm5v$ is initially considered since this is the optimal supply level for this IC process. Accordingly, the full-scale current level of 400 μ A is programmed (Iref₁=1, Iref₀=0 in Figure 3.11). The data shows that the maximum stimulation current associated with D₃-D₀=1111 is less than the 400 μ A target value with the shortcoming common to both the anodic and cathodic current magnitudes. This points to an offset in the desired reference current in the bias circuit, owing to process variation in the fabrication of the linear resistance in Figure 3.11. A solution has been determined to correct this in the next IC revision and is discussed in Section 3.4.



Figure 3.14: Independent amplitude variability of the cathodic phase (experimentally measured)

The linearity of the stimulus current magnitude versus DAC input is a desirable feature in characterizing the effectiveness of electrical stimulation on visual perception. The end-point INL estimate is given by the sum of the DNL errors as:

$$INL = \sum_{k=0}^{14} \left| \left(\frac{i_{(k+1)} - i_{(k)}}{\Delta i_{LSB(ideal)}} - 1 \right) \right|, \tag{3.2}$$

which for the anodic and cathodic currents of Figure 3.17 evaluates to 0.8224 and 0.8085, respectively¹. The tracking between the anodic and cathodic amplitudes exhibits an error that increases with the current magnitude, pointing to a static gain mismatch between the PMOS sourcing and NFET sinking circuits of Figure 3.10. At $D_3-D_0=1111$, the tracking error is 7.24% with respect to the anodic current. The charge imbalance introduced by this mismatch can be neutralized with the charge

¹INL for the ideal straight line is zero.



Figure 3.15: Timing variability with stimulus frequency at 100 frames/second (experimentally measured)

cancellation facility, discussed in Section 3.3.4. Proposed improvements to reduce this in subsequent IC fabrication are discussed in Section 3.4.

Figure 3.18 provides a similar measurement where the supply rails are extended to $V_{dd}/V_{ss}=\pm7v$ to support the delivery of 600μ A full-scale current (Iref₁=1, Iref₀=1) to the 10k Ω load. The INL of the anodic and cathodic phases is computed to be 2.5098 and 0.7277, respectively². The nonlinearity estimate for the anodic current is higher owing to the trailing off of output current approaching D₃-D₀=1111, where PFETs M₁₇ and M₁₈ in Figure 3.10 enter the linear region as the increasing load voltage reduces V_{ds} for these FETs. The anodic to cathodic tracking at $V_{dd}/V_{ss}=\pm7v$ is much worse, exhibiting a percent difference of 26.80% at maximum DAC output current. The reason for this anomalous behavior is not solely a reduced cathodic current as it

²Endpoint INL is measured separately for the anodic and cathodic phases.



Figure 3.16: Timing variability with stimulus frequency at 300 frames/second (experimentally measured)

might appear. Recall, from Figure 3.17 that both current phases are lower that the targeted values, which is also true in Figure 3.18.

The cause of the large mismatch is actually a higher anodic current than should occur with respect to the cathodic current, owing to impact ionization in the transistor due to high V_{ds} . In Figure 3.10, M₇ and M₈ are wide swing connected and the gate of M₉ is connected to a constant potential, *ncas bias*. Thus, the voltage appearing at V_{ds} of M₉ is $V_{dd} - V_{ss} - (V_{ncas,bias} - V_{gs9}) - |V_{gs7}|$ and hence any increase in V_{dd}/V_{ss} directly increments V_{ds} of M₉. High V_{ds} in a transistor results in high electric field in the channel, which imparts excessive energy to the channel electrons especially near the drain region. These high energy electrons generate additional electron-hole pairs due to impact ionization. However, the creation of these new charge carriers in the



Figure 3.17: Anodic and cathodic current amplitudes vs. DAC digital input for V_{dd} =+5v and V_{ss} =-5v (experimentally measured)

channel does not go unbounded as it does in avalanche breakdown and therefore immediate permanent damage does not occur to the device. The holes are attracted to the negatively biased bulk where they appear as a substrate current. The associated electrons from the electron-hole pairs increase the drain current in M₉ [110]. This excessive drain current tracks in M₇ and M₈ and is reflected in the anodic current. Since supply rails of $V_{dd}/V_{ss}=\pm7v$ and beyond are required to support 600 μ A into 10k Ω characteristic load (tissue) impedances [41], extended drain PFETs and NFETs may need to enter into the design of the output stage of Figure 3.10 [108], [111], especially if the fabrication of subsequent generations of the stimulator IC is attempted in process technologies of less than 1.2 μ m gate length or if more than 600 μ A [41] becomes necessary for retinal stimulation using a microchip fabricated in the current


Figure 3.18: Anodic and cathodic current amplitudes vs. DAC digital input for V_{dd} =+7v and V_{ss} =-7v (experimentally measured)

AMI-1.2 μ m CMOS IC process. In the interim however, a design enhancement to correct the problem of the current amplitude mismatch caused by this impact ionization in the 1.2 μ m technology, is proposed in Section 3.4.

3.3.3 DAC current sensitivity to power supply variation

When the chip is powered with the wireless inductive link as indicated in Figure 1.1, it can experience DC supply variations from relative movement between the coils. As noted in [83], such variations can modulate the amplitude of the output stimulus currents directly by offsetting V_{ds} in the current source FETs of Figure 3.10 and indirectly by offsetting V_{gs} in these FETs through a shift in the reference current. The latter is dealt with using a bias circuit exhibiting low sensitivity to supply variation as does the design of Figure 3.11. The former concern is addressed with high impedance current mirrors which were used in Figure 3.10. Figure 3.19 provides a measurement of



Figure 3.19: Anodic/cathodic current amplitude sensitivity to power supply variation (experimentally measured)

the chip's immunity to supply variation over a range of $\pm 4v \leq V_{dd}/V_{ss} \leq \pm 7v$ over the three selectable current ranges of 200μ A, 400μ A, and 600μ A. Supplies of $V_{dd}/V_{ss} = \pm 7v$ are nominal for 600μ A currents into $10k\Omega$ loads, but this already stresses the gate oxides, so the supplies were not pushed beyond these values in Figure 3.19.

The waveforms highlight the increase in anodic current due to impact ionization [110] as discussed in Section 3.3.2, which begins to take effect beyond $V_{dd}/V_{ss}=\pm 5v$. Therefore, it is from the cathodic currents that we assess supply variation immunity for the chip. In the highest selectable current range of 600μ A range, the reduced cathodic current can be supported down to $V_{dd}/V_{ss}=\pm 5v$ at which point the driver circuit loses the headroom to keep its current mirrors saturated³. Over the domain of $\pm 5v \leq V_{dd}/V_{ss} \leq \pm 7v$, the cathodic current in the 600μ A setting shows good immunity

³Apart from the static gain error in the measured bias current leading to reduced current amplitudes, the cathodic current would be 600μ A with minimum supply rails of $V_{dd}/V_{ss}=\pm7$ v.

to supply variation with a measured dependence of 16μ A/V. Likewise, the cathodic currents in the 200 μ A and 400 μ A ranges also show good immunity over $\pm 4v \leq V_{dd}/V_{ss}$ $\leq \pm 7v$ with measured dependences of 4.66μ A/V and 9.33μ A/V, respectively.

3.3.4 Charge cancellation performance

An analysis was performed on the chip to measure the effectiveness of excess charge cancellation. Recall that charge cancellation can be invoked using bit-7 of the 16-bit driver subpacket of Figure 3.4. Also recall that the depletion of charge is logically gated to occur only over the duration of the anodic pulse timing profile selected for the associated driver. In order to evaluate the effectiveness of this capability, the nominal $R_{load}=10k\Omega$ resistance used to model tissue impedance at around 60Hz stimulation [61] is replaced with a capacitance, C_{load} , of the same impedance at 60Hz, or approximately $265nF^4$. Figure 3.20 indicates the nature of the voltage across this load capacitance (top waveform) in response to a biphasic stimulation current (bottom waveform). The DC current supplied to the capacitance during the anodic current phase results in a linearly increasing voltage at the capacitance. Likewise, this voltage linearly decreases due to the cathodic DC current.

Under ideal conditions, an amplitude balanced biphasic current would result in a return of the load voltage to zero at the end of the second phase. However, in Figure 3.20, the *Retina-3.5* stimulator IC is programmed to deliver a biphasic pulse current which is intentionally unbalanced with anodic current of 300μ A and cathodic current of 150μ A, leading to a load voltage which does not return to zero at the end of the stimulation. Thus, excess charge remains on the load capacitance (modeling the electrode) which must be depleted.

In Figure 3.21, the *Retina-3.5* stimulator IC is programmed to implement charge 4 Experimentally modeled discretely with 274nF.



Figure 3.20: No charge cancellation (experimentally measured)

cancellation following the biphasic stimulus pulse from Figure 3.20. Since charge cancellation is commanded in a separate run-time data packet or frame, the effective stimulation rate is now reduced by two as is evident in Figure 3.21. As before, the voltage across the load capacitance charges and discharges linearly in response to the biphasic stimulus current, yet does not return to zero due to the current imbalance.

The third waveform on the lower portion of the display indicates the assertion the a 5ms programmed charge cancellation pulse, during which time PFET M_{23} of Figure 3.10 is engaged by the gate pulldown switch M_{22} . This leads to an R-C discharge of the load capacitance through the resistance of M_{23} as indicated in Figure 3.21. As expected, the duration of the charge cancellation enable pulse (lower waveform) must be sufficiently long to affect a complete removal of any accumulated stray charge on the electrode (or capacitance). Note that the 5ms charge cancellation in Figure 3.21 did not result in complete charge depletion. Therefore, the assertion time has been



Figure 3.21: Short interval of charge cancellation following biphasic stimulation (experimentally measured)

increase to 16.6ms (the complete frame time at 60Hz stimulation rate), as in Figure 3.22 in order to affect a complete removal of stray charge, which is indicated as the output voltage across the load capacitance returns to zero prior to the onset of a subsequent stimulation current pulse. Since a biphasic stimulus current pulse and a charge cancellation event cannot both be scheduled to occur with a single frame, it is recommended that the duration of a requested charge cancellation event be programmed to occupy the entire frame time. This offers the greatest time duration over which charge depletion can take place.

3.3.5 Estimating power requirements of the *Retina-3.5* stimulator IC

Recall that the *Retina-3.5* stimulator IC provides sixty biphasic current outputs for retinal stimulation, with the amplitudes of the anodic and cathodic phases independently programmable for all sixty drivers at 4-bit resolution for each phase. Full-scale



Figure 3.22: Longer interval of charge cancellation following biphasic stimulation (experimentally measured)

currents are programmable at levels of 200μ A, 400μ A, or 600μ A, subject to the extent of retinal deterioration [18]. Pulse timing parameters including start times, pulse widths, and interphas delays are not independently programmable for all drivers, but are instead configurable for each driver from a globally shared programmable memory bank of on-chip timing parameters.

The power consumption associated with operating the micro-stimulator can be accounted for in terms of the power dissipated in the retinal tissue (referred to as the *Load*) plus the additional power overhead required by the micro-stimulator IC. This is expressed mathematically in Equation 3.3 for instantaneous power as a function of time, where the superscript "60" in parentheses refers to the case where all sixty stimulation channels are active. The subscripts *chip*, *load*, and *consumed* refer to the power consumed in the micro-stimulator IC, retinal-tissue, and of the combined

system, respectively.

$$P_{consumed}^{(60)}(t) = P_{chip}^{(60)}(t) + P_{load}^{(60)}(t)$$
(3.3)

Since the total power consumption is formulated as a sum, further derivation will proceed with the power estimates expressed as average quantities. This is justified because the average represents a linear operator in that it distributes correctly across the sum as in Equation 3.4. This is not the case when instantaneous power is expressed as an RMS quantity as in Equation 3.5.

$$\frac{1}{T} \int_0^T P_{consumed}(t) dt = \frac{1}{T} \int_0^T P_{chip}(t) dt + \frac{1}{T} \int_0^T P_{load}(t) dt$$
(3.4)

$$\sqrt{\frac{1}{T} \int_0^T P_{consumed}^2(t) dt} \neq \sqrt{\frac{1}{T} \int_0^T P_{chip}^2(t) dt} + \sqrt{\frac{1}{T} \int_0^T P_{load}^2(t) dt}$$
(3.5)

3.3.5.1 Power dissipated in the retinal stimulator IC

Some of the industry standard circuit-level simulators such as *Hspice* are capable of estimating dissipated power in extracted IC layouts. However, as the *Retina-3.5* stimulator IC layout contains nearly 70000 FETs, chip level simulations which cover milliseconds of real time are impractical. Fortunately, in the case of the *Retina-3.5* IC, the array of sixty identical output drivers accounts for about 75% of the die area. Therefore, an accurate estimate of the dissipated power of the chip can be formulated from a simulation of a single output driver (one from the array of sixty), the biasing circuit (which manifests static power dissipation), and the digital section (associated with packet synchronization and timing generation) as illustrated in Figure 3.23.

The single output driver, biasing circuit, and digital section from Figure 3.23 are designated as subcircuits, X1, X2, and X3, respectively. In simulation, the output driver of subcircuit X1 is loaded with a resistance $R_{load} = 10k\Omega$ to model retinal



Figure 3.23: Layouts of the *Retina-3.5* stimulator IC which are simulated in *Hspice* to determine power dissipation

impedance [61]. The power dissipation of the chip could be predicted from the simulated estimates of subcircuits X1, X2, and X3, designated P_{X1} , P_{X2} , and P_{X3} , respectively, as in Equation 3.6, excluding the power, P_{load} , dissipated in R_{load} which is off chip.

$$P_{chip(3D^5)} = 60 \left(P_{X1} \right) + P_{X2} + P_{X3} \tag{3.6}$$

⁵The subscript substituent, "(3D)", indicates that this is the power associated with the three

In calculating the power requirements of the micro-stimulator, the biphasic stimulus current pulse of Figure 3.24 is considered [18]. The micro-stimulator is programmed to produce several variations in current amplitude, pulse repetition rate, and pulse widths, which are annotated as A, W, and T, respectively, on the stimulus waveform of Figure 3.24. Balanced anodic and cathodic current amplitudes of $400\mu A$ at $V_{dd}/V_{ss} = \pm 5v$ (the typical case) and $600\mu A$ at $V_{dd}/V_{ss} = \pm 7v$ (the worse or maximum case) for *Retina-3.5* are considered representative for retinal stimulation [18]. Pulse repetition rates of 50Hz and 60Hz are considered in keeping with results of flicker fusion experiments reported in [18]. Anodic and cathodic pulse widths and interphase delay were kept equal and varied among 1ms, 2ms, and 3ms, consistent with stimulation experiments also reported in [18].



Figure 3.24: Parameters of the biphasic current stimulus pulse

The subcircuits of Figure 3.23 were programmed to produce the biphasic stimulus current pulse of Figure 3.24 in each of the parametric combinations described (twelve cases in all). Subsequently, *Hspice* simulations were conducted to estimate the power dissipation of *Retina-3.5* when operating in each case. The results are tabulated in Table 3.2.

dimensional model of the chip. This is in contrast to $P_{chip(2D)}$ to be introduced in Chapter 5, which is associated with a two dimensional model of the chip used in numerical thermal simulations.

V_{dd} ,	current	frame	pulse	bias	driver	load	driver	load	digital	chip
Vss	$(^{1,2})$	rate	width	power	power	power	$power \times 60$	$power \times 60$	power	$power^3$
	Α	$f = \frac{1}{T}$	W	P_{X1}	P_{X2}	Pload	$P_{X2} \times 60$	$P_{load} \times 60$	P_{X3}	$P_{chip(3D)}$
$[V_{DC}]$	$[\mu A]$	[Hz] ¹	[ms]	[mW]	[mW]	[mW]	[mW]	[mW]	[mW]	[mW]
+5, -5	400	50	1	2.4700	0.1041	0.1633	6.2436	9.8004	0.4726	9.1862
+5, -5	400	50	2	2.4700	0.2036	0.3251	12.2154	19.5066	0.4726	15.1580
+5, -5	400	50	3	2.4700	0.3041	0.4884	18.2448	29.3070	0.4726	21.1874
+5, -5	400	60	1	2.4700	0.1243	0.1951	7.4562	11.7030	0.4750	10.4012
+5, -5	400	60	2	2.4700	0.2443	0.3901	14.6568	23.4066	0.4750	17.6018
+5, -5	400	60	3	2.4700	0.3643	0.5852	21.8568	35.1102	0.4750	24.8018
+7, -7	600	50	1	3.5647	0.2043	0.3310	12.2604	19.8618	0.4964	16.3216
+7, -7	600	50	2	3.5647	0.3962	0.6589	23.7696	39.5310	0.4964	27.8308
+7, -7	600	50	3	3.5647	0.5899	0.9899	35.3916	59.3928	0.4964	39.4527
+7, -7	600	60	1	3.5647	0.2441	0.3953	14.6448	23.7174	0.5017	18.7112
+7, -7	600	60	2	3.5647	0.4754	0.7906	28.5228	47.4354	0.5017	32.5892
+7, -7	600	60	3	3.5647	0.7067	1.1859	42.4008	71.1540	0.5017	46.4672

Table 3.2: *Hspice* simulated power dissipation for the *Retina-3.5* micro-stimulator resulting from variations in parameters of the biphasic stimulus current pulse

¹Anodic and cathodic current amplitudes resulting from *Hspice* simulation at $V_{dd}/V_{ss} = \pm 5v$ were $\pm 400.8\mu$ A and -405.1μ A, respectively

²Anodic and cathodic current amplitudes resulting from *Hspice* simulation at $V_{dd}/V_{ss} = \pm 7v$ were $\pm 575.3\mu$ A and -572.1μ A, respectively. The driver output stage of Figure 3.10 transitions from saturation to the linear region when attempting to provide 600μ A for $R_{load} = 10k\Omega$ [61] with $V_{dd}/V_{ss} = \pm 7v$. Therefore, actual currents fall short of the requested values (see Figure 3.18). ³Excludes load power

When computing power estimates on semiconductor circuits Hspice considers only the power lost, or dissipated. Accordingly, the estimates of $P_{chip(3D)}$ from Table 3.2 are taken as losses which would give rise to heat. Therefore, these values of $P_{chip(3D)}$ are used to compute the power densities, $P_{chip(3D)}^{(density)}(i, j, k)$ and $P_{chip(2D)}^{(density)}(i, j)$, based on derivations in Section 5.5.2 of Chapter 5 for use in the numerical *bio-heat* formulations of Equations 5.53 and 5.55, respectively, developed in Section 5.2.2 of Chapter 5 to predict temperature increase in the 2D head/eye model. The results of these thermal simulations are summarized in Table 5.12 of Chapter 5 with the waveform parameters for the associated values of $P_{chip(3D)}$ retabulated. The biphasic stimulus current pulse represents a waveform for which the average power can be easily calculated analytically. Provided that the current is delivered to a resistive load, R_{load} , the expected

V_{dd} ,	current	frame	pulse	simulated	theoretical	% difference
V_{ss}		rate	width	load power ¹	load power ²	W.R.T. theo-
	Α	$f = \frac{1}{T}$	W	P _{load,simulated}	$P_{load, theoretical}$	retical value
$[V_{DC}]$	$[\mu A]$	[Hz]	[ms]	[mW]	[mW]	
+5, -5	400	50	1	0.1633	0.1600	2.06
+5, -5	400	50	2	0.3251	0.3200	1.59
+5, -5	400	50	3	0.4884	0.4800	1.75
+5, -5	400	60	1	0.1951	0.1920	1.61
+5, -5	400	60	2	0.3901	0.3840	1.59
+5, -5	400	60	3	0.5852	0.5760	1.60
+7, -7	600	50	1	0.3310	0.3600	8.06^{-3}
+7, -7	600	50	2	0.6589	0.7200	8.49^{-3}
+7, -7	600	50	3	0.9899	1.0800	8.34 ³
+7, -7	600	60	1	0.3953	0.4320	8.50^{-3}
+7, -7	600	60	2	0.7906	0.8640	8.50^{-3}
+7, -7	600	60	3	1.1859	1.2960	4.98 ³

 Table 3.3: Comparison of simulated and theoretical load power

¹Duplicated from Table 3.2

²Calculated using the theoretical formulation $P_{load} = 2fWA^2R_{load}$, where $R_{load} = 10k\Omega$ [61].

³Increased percent difference for the $V_{dd}/V_{ss} = \pm 7v$ cases, is due to the inability of *Retina-3.5* to attain to 600μ A when loaded with $R_{load} = 10k\Omega$ [61] for $V_{dd}/V_{ss} = \pm 7v$ (see footnote #2 from Table 3.2 and Figure 3.18).

average power can be formulated as

$$P_{load} = \frac{1}{T} \int_0^T i_{load}^2(t) R_{load} dt = \left(\frac{i_{load}}{\mathbf{R}_{MS}}\right)^2 R_{load} = \frac{2R_{load}}{T} \int_0^W A^2 dt = \frac{2WA^2 R_{load}}{T}, \quad (3.7)$$

where the parameters A, W, and T are defined as in Figure 3.24 and the load resistance is defined as $R_{load} = 10 \mathrm{k}\Omega$ [61]. Therefore, in order to provide a measure of confidence in the simulated power estimates in Table 3.2, a comparison of the simulated and theoretical values for the load power is given in Table 3.3. The increased percent difference for the $V_{dd}/V_{ss} = \pm 7\mathrm{v}$ cases is due to the inability of *Retina-3.5* to attain to $600\mu\mathrm{A}$ when loaded with $R_{load} = 10\mathrm{k}\Omega$ [61] for $V_{dd}/V_{ss} = \pm 7\mathrm{v}$ (see footnote #2 from Table 3.2 and Figure 3.18).

3.3.5.2 Power consumption in the retinal stimulator IC

In order to provide further validation for the estimates of power obtained from *Hspice* simulation of the IC layout, an experimental measurement of the power consumption and dissipation is performed. The *Retina-3.5* micro-stimulator operates from dual DC supply rails of V_{dd} and V_{ss} to produce the anodic and cathodic phases, respectively, with respect to a central ground return, designated *Gnd*. Therefore, the left hand side of Equation 3.3 can be expressed as a power consumption by expanding $P_{consumed}^{(60)}(t)$ as in Equation 3.8 (now expressed as an average).

$$P_{consumed}^{(60)} = \frac{1}{T} \int_0^T P_{consumed}(t) dt = \frac{1}{T} \int_0^T v(t) i(t) dt = V_{dd} I_{dd}^{(60)} + V_{ss} I_{ss}^{(60)}, \qquad (3.8)$$

where I_{dd} and I_{ss} are the average supply currents for the V_{dd} and V_{ss} supplies. The experimental setup for measuring power consumption according to this formulation is illustrated in Figure 3.25. A small series resistance of value $R_{series} = 10.3\Omega$ is connected to V_{dd} and V_{ss} in order to provide a measure of supply currents, I_{dd} and I_{ss} , from each rail. Subsequently, the expression for power consumption is expanded as in Equation 3.9.

$$P_{consumed}^{(60)} = V_{dd} \left(\frac{(\Delta V_{dd}^{(60)})}{R_{series}} \right) + V_{ss} \left(\frac{(\Delta V_{ss}^{(60)})}{R_{series}} \right)$$
(3.9)

Load currents are observable across the resistances used to model the retinal tissue impedance at these stimulation frequencies, again defined as $R_{load} = 10k\Omega$ [61]. I_{dd} and I_{ss} are measured for $V_{dd}/V_{ss} = \pm 5v$. Measured load power is formulated as

$$P_{load}^{(60)} = 60 \frac{\overbrace{(v_{load})^2}^{\text{RMS}}}{R_{load}}$$
(3.10)

Subsequently, micro-stimulator power can be inferred as the difference in power



Figure 3.25: Experimental setup for measuring power consumption in the *Retina-3.5* stimulator IC (implant)

consumption and power dissipated in the loads, as given in Equation 3.11.

$$P_{chip}^{(60)} = P_{consumed}^{(60)} - P_{load}^{(60)}$$
(3.11)

The results of the measurement experiment along with the inferred micro-stimulator power are summarized in Table 3.4. The data shows that the experimental measurements are in good agreement with the simulated values, thus validating these estimates for characterization of stimulator power dissipation, especially for the study of thermal response of the retinal prosthesis presented in Chapted 5.

3.3.6 Measurement summary and die photo

The measurements for the stimulator IC are summarized in Table 3.5. A die photograph of the *Retina-3.55* stimulator IC is given in Figure 3.26. The chip was implemented in the AMI-1.2 μ m two-metal, two-poly CMOS process through the MOSIS facility, with die circuit area dimensions of 4.6mm×4.7mm. A peripheral ring of 104 100 μ m×100 μ m pads encloses the stimulator core. Power and control signal pads are allocated along the bottom edge of die to simplify connection to a separate adjacent

Table 3.4: Experimentally measured power consumption and dissipation for the *Retina-3.5* micro-stimulator resulting from variations in parameters of the biphasic stimulus current pulse

V_{dd} ,	current	frame	pulse	measured	measured	inferred	simulated	% difference
V_{ss}^{1}	$(^{2})$	$rate^3$	$width^4$	$consumption^5$	load power	chip power ⁶	chip power ⁷	W.R.T.
	А	$f = \frac{1}{T}$	W	$P_{system}^{(60)}$	$P_{load}^{(60)}$	$P_{chip}^{(60)}$	$P_{chip(3D)}$	simulated
$[V_{DC}]$	$[\mu A]$	[Hz]	[ms]	[mW]	[mW]	$[m\hat{W}]$	[mW]	value
+5, -5	400	50	1	18.4818	11.3276	7.1541	9.1862	22.12
+5, -5	400	50	2	36.4597	20.8378	15.6219	15.1580	3.06
+5, -5	400	50	3	53.0817	28.7304	24.3513	21.1874	14.93
+5, -5	400	60	1	22.4489	11.6612	10.7877	10.4012	3.72
+5, -5	400	60	2	42.7871	22.8569	19.9302	17.6018	13.23
+5, -5	400	60	3	61.2672	33.6595	27.6076	24.8018	11.31

¹Due to a shortcoming in *Retina-3.5* operation at $V_{dd}/V_{ss} = \pm 7v$ (see the anodic and cathodic current mismatch of Figure 3.18), the experimentally measured power consumption and dissipation for validation with the results of Table 3.2 were conducted only for the cases of $V_{dd}/V_{ss} = \pm 5v$.

²Anodic and cathodic pulse amplitudes measured experimentally at $V_{dd}/V_{ss} = \pm 5v$ were 400µA and -408µA, respectively.

 3 Because stimulus timing is derived from a 12MHz master clock on the extraocular FPGA processor, actual frame rates are 49.827Hz and 60.048Hz, rather that 50Hz and 60Hz, respectively.

⁴Because stimulus timing is derived from a 12MHz master clock on the extraocular FPGA processor, actual pulse widths are 1.023ms, 2.046ms, and 2.991ms at 50Hz stimulation and 1.045ms, 2.025ms, and 3.004ms at 60Hz stimulation, rather than 1ms, 2ms, and 3ms, respectively.

⁵The series resistance, $R_{series} = 10.3\Omega$, from Figure 3.25 is used to measure source currents, I_{dd} and I_{ss} . The associated power dissipations, $\frac{(\Delta V_{dd})^2}{R_{series}}$ and $\frac{(\Delta V_{ss})^2}{R_{series}}$, are negligible and therefore not included in these measurements.

⁶Inferred using $P_{chip}^{(60)} = P_{consumed}^{(60)} - P_{load}^{(60)}$

⁷Duplicated from Table 3.2

Technology	MOSIS $1.2\mu m$ CMOS
Physical die size	5.5 mm $\times 5.25$ mm
Circuit area size	$4.7\mathrm{mm} \times 4.6\mathrm{mm}$
Number of current generators	60
Number of electrodes	60
Maximum clock rate	$1.5 \mathrm{~Mhz}$
Maximum frame rate	1465 frames/second
Frame size	1024 bits
Amplitude resolution	4-bits, 3 full
	scale settings
Timing resolution	4 clock cycles, or
(edge placement)	1/256 of the frame time
Power consumption	$50 \mathrm{mW}$
Anodic current	0.8224
nonlinearity (INL)	
Cathodic current	0.8085
nonlinearity (INL)	
Anodic/Cathodic tracking	7.24%
Supply sensitivity	$16\mu A/V$

 Table 3.5: Chip performance specification and measurements

IC (not discussed here) providing power carrier rectification, filtering, and supply regulation⁶. The sixty biphasic stimulus current output pads (numbered 1-60) are distributed along the remaining three sides of the die.

 $^{^6{\}rm Continued}$ development of the stimulator IC design for inclusion of inductive telemetry for wireless power and data transfer would lead to integration of the carrier rectifier and filtering and supply regulation curcuits in the stimulator IC



Figure 3.26: Die micrograph of the *Retina-3.55* micro-stimulator IC

3.4 Design enhancements

A number of limitations have been identified in the *Retina-3.5/Retina-3.55* stimulator IC's which provide opportunities for improvement in subsequent design iterations. Section 3.3.2 indicates the need for improved circuit design in the biphasic amplifier output stage of Figure 3.10 in order to overcome poor matching at $V_{dd}/V_{ss}=\pm7v$ and beyond. Recall that since M_7 and M_8 form a diode connected reference, the drain voltage of M_8 will not deviate strongly from V_{dd} as a function of drain current. Therefore, most of the 14v drop from V_{dd} to V_{ss} occurs across M_9 . A proposed a solution to eliminate the associated impact ionization is to introduce a number of diode-connected NFETs between M_8 and M_9 to absorb some of the voltage drop. This will not increase power dissipation since the voltage across and current through the transistor stack is unchanged.

Another enhancement to the driver circuit of Figure 3.10 to further improve pulse amplitude matching is to use a single DAC with a multiplexed digital input code instead of separate DACs with dedicated input codes for the anodic and cathodic pulses. This will ensure that the same DAC current is used for both pulses and will remove the negative effects of process variation from this portion of the design. Trading one DAC for a digital 4-bit 2-to-1 multiplexer is not expected to require additional area over the present implementation of two separate DACs. This enhancement has been implemented in the *Retina-4* prototype IC discussed in Chapter 4 with the improve driver circuit shown in Figure 4.6.

The bias circuit of Figure 3.11 suffered a lower than expected reference current because the linear resistance was fabricated at a higher value than designed. This can be improved upon in the next IC revision by employing a digital resistance which can be programmed using a small set of unused data bits in the configuration packet format of Figure 3.2, thereby offering the means to tune out process variation on the bias circuit, or even to globally adjust output currents beyond 600μ A subject to the limits of the supply rails. This solution is also implemented in the *Retina-4* prototype chip discussed in Chapter 4.

There are two issues involving the charge cancellation mechanism which can be improved in the next IC design. The present implementation in the *Retina-3.5* and *Retina-3.55* stimulator ICs requires that a separate run-time data frame be used to program the occurrence of a stray charge removal event, during which time a biphasic stimulus current pulse cannot also be programmed to occur concurrently within the same frame. As such, this reduces the achievable stimulation imaging rate by a factor of two if charge cancellation is performed after every biphasic stimulation pulse. This can be easily remedied with no additional area or processing overhead by allocating one of the eight timing profiles to be used only for scheduling the charge cancellation event, while the remaining seven timing profiles continue to serve in anodic/cathodic pulse scheduling and timing. Accordingly, the two pulse phases as well as a charge cancellation event can be scheduled during a single image frame time. This obviously imposes a constraint on the time duration available for the charge cancellation enable pulse to be active, for a constant frame time, where the prior recommendation was to perform charge cancellation over the full duration of the frame time. The reduced available time can be compensated by widening the shorting PFET switch, M_{23} , in the biphasic amplifier of Figure 3.10, thereby lowering its resistance path to ground. Accordingly, this decreases the R-C discharge time constant and speeds the removal of stray charge from the electrode output.

In Figure 3.21, the exponential decay of the load capacitance voltage from 1.34v to 320mv (red waveform) over the 5.094ms cancellation interval (blue waveform) implies an approximate discharge resistance $R_{M_{23}}$ for PFET M₂₃ of about 13k Ω . This yields

the classical first-order R-C circuit with discharge time given by:

$$t_{\rm discharge} \approx -R_{\rm M_{23}} C_{\rm load} \ln\left(\frac{v_{\rm f}}{v_{\rm i}}\right) \approx -R_{\rm M_{23}} C_{\rm load} \ln\left(\frac{v_{\rm f} C_{\rm load}}{I_{\rm mismatch} \Delta t_{\rm pw}}\right)$$
(3.12)

where $C_{\text{load}} \approx 274 \text{nF}$, $R_{\text{M}_{23}} \approx 13 \text{k}\Omega$, I_{mismatch} is the DC imbalance between anodic and cathodic phases, Δt_{pw} is the anodic/cathodic pulse widths, v_{i} is the initial voltage associated with residual charge prior to charge cancellation, and v_{f} is the desired final DC voltage on the electrode (ideally zero).

For example, with PFET M_{23} minimally sized as is the case for the *Retina-3.5* and *Retina-3.55* stimulator ICs, the time required to deplete the residual charge introduced from 10μ A of amplitude imbalance from 2ms anodic and cathodic pulses to a level of 1mV would be 15.3ms. Similarly, discharging to a voltage level of 10mv would require 7.1ms, in which case nearly 9.6ms of time remain for the anodic and cathodic pulse widths and the interphase delay to be scheduled into a single 16.66ms frame time at 60Hz stimulation rate. Otherwise, PFET M_{23} could be widened more to further lower the discharge time, in order to allocate more time to the anodic and cathodic phases of the biphasic stimulation pulse current.

3.5 Summary

An implantable micro-stimulator has been presented for use in an epi-retinal prosthesis system. The stimulator IC is designed and implemented in AMI–1.2 μ m CMOS. It is programmable in real-time from external prosthesis hardware with configuration data and run-time image data at frame-rates up to several hundred images/sec. Sixty unmultiplexed stimulus driver circuits can be programmed with independent pulse amplitudes to represent images intensities consistent with acquired data such as from an external mini-camera. Globally shared pulse timing parameters are also programmable. Error detection mechanisms including cyclic redundancy check and checksum calculations are implemented on-chip to strengthen robust communication of stimulus instructions.

Chapter 4

Improvements in micro-stimulator area utilization

4.1 Introduction

As discussed in the opening section of Chapter 3, several neuro-stimulator devices intended for implantation have been designed and fabricated for electrical stimulation of tissues. However, these stimulators use DAC structures whose areas scale exponentially (2^n) with the bit width, n. An alternative DAC structure targeted for stimulator arrays on implantable neuro-stimulators is introduced here, in which the implementation area scales linearly with bit width, n, instead of exponentially. This would yield more stimulus circuits for the same chip area and subsequently greater spatial resolution in stimulation. Also introduced is a programmable biasing circuit, DAC gain prescalar, and DC offset circuit in order to facilitate device tuning in the presence of variations in retinal degradation per patient. Each of these circuits are digitally tunable in order to benefit from serial communication protocols conducive for wireless inductive [78] or optical [33], [112] telemetry links. This provide the means to adjust the DAC's effective stimulus current range so as to optimally meet the needs of individual patients.

4.2 Motivation

In the development of the cochlear prosthesis it has been determined that six electrodes present sufficient information for a patient to learn to conduct a telephone conversation [18]. Subsequently, a number of psycho-physical studies have been conducted involving pixelated imaging hardware to investigate the effectiveness of low resolution vision [102]–[104]. Figure 4.1 provides an example of what pixelated vision might offer at 8×8 spatial resolution consistent with the capabilities of the *Retina-3.5* stimulator IC as well as some projections of how vision might improve with a greater number of pixels and associated stimulus circuits.



(a) 320 x 320, 8-bit grayscale (b) 8 x 8, 8-bit grayscale (c) 32 x 32, 4-bit grayscale (d) 32 x 32, 8-bit grayscale

Figure 4.1: Low-resolution vision simulated from spatially subsampled and grayscale subsampled images

In an additional study reported in [53], experiments were conducted to characterize low-resolution vision in terms or the number of electrodes, size and spacing of electrodes, the number of gray-levels (which translates to DAC bit width), as well as the electrode dropout percentage (related to current driver circuits on the stimulator IC which might suffer manufacturing defects or otherwise become inoperable). Results indicate that increased electrode size/spacing for fixed spatial resolution increases the difficulty in detecting facial features. It was also apparent that only two gray levels (essentially, a binary image) were insufficient for resolving facial detail. An important discovery from this study, was that "scanning" or movement of the "vision window" across the scene could partially overcome "tunnel vision" which occurs when the number of pixels is reduced for fixed electrode size. However, this is exacerbated when increasing the pixel dropout percentage. Based on these insights, circuit topologies which might exploit finite silicon area to gain either greater spatial resolution or greater intensity resolution would be relevant and valuable to a retinal prostheses. Thus, efforts to significantly reduce DAC size would appear to be well-justified in order to raise stimulation resolution in a given chip area. This has motivated the development of the *multi-bias* DAC.

Of the stimulator ICs which have been designed for use in prostheses, most of them employ current-mode digital-to-analog converters. One of the popular types of DAC structures which is consistently used is the binary-weighted, or current scaled, converter, which operates by selectively summing multiples of (or fractions of) a reference current in prescaled powers of two. An example of this type of converter is shown in Figure 4.2 for the case of simple current mirrors.



Figure 4.2: Conventional 8-bit binary-weighted current-mode DAC using simple PMOS current mirrors

Although this DAC does not yield DNL and monotonicity as good as the thermometercoded DACs [113]–[115], and requires essentially the same amount of analog circuitry [116], the DAC boasts the advantage of requiring no circuit overhead for decoding the digital input, which likely justifies its popularity in implantable stimulators where area is a premium. The tracking performance between the reference and mirror sides of the current mirrors can suffer from differences in V_t or shifts in device geometry due to process variation, or from channel length modulation [117]. These effects can lead to non-monotonicity in the DAC staircase characteristic [118]. For currents i_1 and i_0 in Figure 4.2 the ratio is given as:

$$\frac{\mathbf{i}_1}{\mathbf{i}_0} = \frac{\left(\frac{\mu_n C_{ox}}{t_{ox}}\right) \left(\frac{2W}{L}\right) (V_{gs} - V_t)^2 (1 + \lambda V_{ds_1})}{\left(\frac{\mu_n C_{ox}}{t_{ox}}\right) \left(\frac{W}{L}\right) (V_{gs} - V_t)^2 (1 + \lambda V_{ds_0})}$$
(4.1)

Robust analog layout techniques address the process variation affecting device matching [119]. Furthermore, increased output impedance through cascoding can minimize current mismatch induced from differences in channel length modulation experienced between the referenced and mirrored branches. This reduces the ratio of Equation 4.1 to purely a geometric relation. The obvious disadvantage of the binary weighted DAC (or of the thermometer-coded DAC) is that implementation area grows rapidly with increases in resolution.

In [120], a DAC implementation is reported in which the active area is reduced to 0.01mm^2 in $1.2\mu\text{m}$ for 5-bit resolution. This form of reduced area DAC is also targeted for implantable stimulators, and therefore provides for programmable pulse amplitudes for anodic and cathodic stimulus phases. Instead of increasing the transistor widths in powers of two at fixed length across each DAC branch as described for the conventional binary weighted DAC, the device widths and lengths are varied together in powers of two in order to achieve the same relative current weighting. Unfortunately, this does not yield device tracking as robust compared with multiply instantiating transistors of fixed width and length [109]. Thus, this implementation comes at the expensive of INL and DNL, which could introduce non-monotonicity into the DAC characteristic, as described in [118]. The *multi-bias* DAC seeks to offers an alternative to these implementations styles in which transistors of fixed width and length are used in a low area topology while still attempting to retain a lower DAC INL and DNL.

This chapter is organized into five major sections. Section 4.3 introduces the novel concept of the *multi-bias* DAC and how this leads to a lower implementation area over conventional current mode DACs. Section 4.4 presents the prototype IC for the *multi-bias* concept with discussions of functionality and design issues. Simulation and measurement results are presented in Section 4.5. Section 4.6 covers means of improvement in successive iterations, with concluding remarks in Section 4.7.

4.3 Proposed Improvement: The Mutli-bias DAC

Currents in the binary-weighted DAC derive from a common FET gate bias produced in the reference branch, labeled V_{ref} in Figure 4.2. This is distributed across the DAC branches to reproduce the output currents. Therefore, relative binary weightings of currents are controlled using device geometries and are defined as

$$\mathbf{i}_n = K \frac{2^n W}{L} (V_{ref} - V_t)^2, \qquad (4.2)$$

for $0 \leq n < N$ (ignoring channel length modulation associated with finite output impedance). For an N-bit DAC of simple current mirrors, this requires $2^N - 1$ transistors of size $\frac{W}{L}$, assuming a robust analog layout technique as described in [109]. The modification developed for the *multi-bias* DAC is to replace the single FET gate bias, V_{ref} , with multiple gate biases, $(V_{bias_0}, V_{bias_1}, ..., V_{bias_{N-1}}$ for an N-bit DAC) with N transistors all sized at $\frac{W}{L}$ instead of $2^N - 1$ transistors sized at $\frac{W}{L}$. Then, the drain currents for the N-bit DAC become

$$i_n = K \frac{W}{L} (V_{bias_n} - V_t)^2.$$
 (4.3)

This new technique is referred to as the *multi-bias* DAC, because each DAC branch uses an independent FET gate bias. Hence, relative currents are controlled by gate bias rather than by geometry. This permits each branch to use identically sized devices, which is the key to area reduction while preserving device tracking, as shown in Figure 4.3a for an 8-bit DAC.

The biases are generated using currents reflected into diode connected FETs with the aid of a conventional binary weighted DAC, as shown in Figure 4.3b. Although this second DAC might appear to defeat the purpose of the *multi-bias* DAC because of its high area penalty, it is instantiated only once per chip to service a much larger array of reduced area stimulus circuits based on *multi-bias* concept. The bias voltages, $V_{bias_0}-V_{bias_{N-1}}$, are therefore generated centrally and distributed to all of the DACs throughout the micro-stimulator.

4.4 The prototype *multi-bias* DAC chip

4.4.1 Architecture

A system block diagram of the prototype *multi-bias* DAC chip is presented in Figure 4.4. The stimulus circuits are programmed through a simple serial digital interface consisting of *clock* and *data* input pins. The chip processes two types of formatted data packets, designated as either *configuration* data or *stimulus* data. Serial digital data is shifted into a 15-bit fifo on each cycle of the clock input, after which it is latched into either an 11-bit stimulus data register upon assertion of the *load-config* digital input pin.



Figure 4.3: Multi-bias DAC concept introduced with simple PMOS current mirrors

Bits (10-3) of the stimulus data register are allocated as digital input to an 8-bit *multi-bias* stimulus DAC (discussed in subSection 4.4.2). The current outputs from the stimulus DAC and the DC offset DAC are summed and reflected into the biphasic output amplifier. Bits (2-0) of the stimulus data register affect current steering within the output amplifier (discussed in subSection 4.4.3), to produce either an anodic or cathodic current pulse.

Bits (14-8) of the configuration data register are allocated for tuning the programmable bias circuit (discussed in subSection 4.4.4). Bits (7-4) are reserved for



Figure 4.4: System block diagram for the reduced area *multi-bias* DAC prototype chip

programming the current gain prescalar (discussed in subSection 4.4.5.1), and bits (3-0) are set aside for programming the *multi-bias* DC offset DAC (discussed in Section 4.4.5.2).

4.4.2 Multi-bias stimulus DAC

The 8-bit *multi-bias* DAC implemented at the position shown in the block diagram of Figure 4.4, with its 8-bit digital input taken from bits $(D_7 - D_0)$ of the stimulus data register. The resistive load shown in Figure 4.3a represents the loading of the biphasic output amplifier, to which the *multi-bias* DAC delivers its output current, i_{DAC} . Since the output amplifier operates between a positive V_{dd} and a negative V_{ss} , the power rails of the *multi-bias* DAC are level-shifted from V_{dd}/Gnd to Gnd/V_{ss} .

INL and DNL in the transfer characteristic of the *multi-bias* DAC as well as with the conventional binary weighted DAC are sensitive to correctly scaled currents in the DAC branches. In both DACs, each branch current, i_k , associated with digital input bit, D_k , should be twice the magnitude of branch current, i_{k-1} . Therefore, the performance of wide swing cascoded and fully cascoded forms of the *multi-bias* DAC as well as the DAC based on simple current mirrors, introduced in Figure 4.3a, has been investigated.

The wide swing cascoded form of the *multi-bias* DAC is shown in Figure 4.5. This structure provides increased output impedance in the mirrors of the DACs and will be shown to give improved current matching, while requiring only one additional bias to be distributed to the DACs (eight for the DAC current sources and one for the cascode bias). This is the form of the DAC implemented on the prototype chip with simulated and measured results given in Section 4.5. Note that the lower compliance voltage available with the wide swing current mirrors, while offering potential improvements in power consumption, is not the primary motivation for considering a wide swing topology, but rather the higher output impedance at the cost of a single additional bias.

4.4.3 Biphasic output current amplifier

The currents i_{DAC} and i_{offset} from the *multi-bias* and DC offset DACs, respectively, are summed and passed into the biphasic current amplifier as shown in the block diagram from Figure 4.4. This amplifier acts as an output stage to drive the tissue impedance and is detailed in Figure 4.6.

The current from the DACs is passed into NFETs M_1 and M_2 , which form the



Figure 4.5: Wide swing cascoded, 8-bit *multi-bias* DAC

reference branch of a wide swing cascode mirror formed with M_5 and M_6 (for producing the anodic pulse) and with M_9 and M_{10} (for producing the cathodic pulse). NFETs M_9 and M_{10} are 30 times wider that M_1 and M_2 in order to scale the full-scale $20\mu A$ from the stimulus and offset DACs up to full-scale level of $600\mu A$ [41]. The current mirrored into NFETs M_5 and M_6 is passed to M_3 and M_4 which form the reference branch of a V_{dd} -referenced wide swing cascode current mirror. This current is mirrored to M_7 and M_8 which subsequently sources current to the load (tissue) impedance. PFETs M_7 and M_8 are also 30 times wider that M_3 and M_4 in order to achieve $600\mu A$ [41]. The gate of current source NFET M_6 is switchable to either the gate potential of M_2 or to the V_{ss} rail to either enable or disable the anodic pulse, respectively. In the latter case, current flow in M_3 , M_4 , M_5 , M_6 , M_7 , and M_8 would be cut off. This occurs under the control of complementary logic signals A and \overline{A} , which transition between the V_{ss} rail (logic-0) and the V_{cc} rail (logic-1). The circuit



Figure 4.6: Biphasic current output amplifier

implementation of the complementary switches is provided in the inset schematic of Figure 4.6. Similarly, the gate of current source NFET M_{10} is switchable to either the gate potential of M_2 or to the V_{ss} rail to either enable or disable the cathodic pulse, respectively. When disabled, current flow in M_9 and M_{10} is cut off. This occurs under the control of complementary logic signals C and \overline{C} .

Since this output stage is intended for use in the epi-retinal prosthesis, the electrode impedance and retina impedance are modeled with the load resistance, R_{LOAD} . Although the value of this load varies with the geometry of the electrode, extent of retinal degeneration, and frequency of stimulation, impedances on the order of $10k\Omega$ have be observed experimentally [61]. Wide swing cascode current mirrors are used in the output stage to achieve maximize output current per supply voltage while maintaining FET operation in the saturation region [116]. NFETs M_{11} , M_{12} , and M_{13} form a charge cancellation circuit which can be used to neutralize the accumulation of charge on the electrode, resulting from finite mismatch between the PMOS and NMOS mirrors of the biphasic driver. Charge cancellation should be performed so as to not overlap in time with the anodic and cathodic phases of the stimulus pulse. PFET M_{13} is intended to provide a path to ground (the return potential) in order to effectively short circuit any stray charge on the electrode output. PFET M_{13} is turned on using pull-down device M_{12} under the control of logic signal "charge-cancel". Since logic signal transitions are confined between V_{ss} and Gnd, PFET M_{13} is cutoff using passive diode-connected PFET M_{11} , acting as a weak pull-up to V_{dd} .

4.4.4 Tunable bias circuit

The core of the biasing circuit for the prototype chip is derived from the self-biasing (or *Bootstrap reference*) circuit [121] used in the *Retina-3* stimulator IC [83]. It is also used in the biasing circuits in the *Retina-3.5* and *Retina-3.55* stimulator ICs as illustrated from Figure 3.11. Shown in Figure 4.7, this circuit establishes a reference current through the intersection of the linear I-V relationship of resistance R_{bias} (chosen at 50k Ω) with the quadratic I-V characteristic of NFET M₁. This provides a reference which is independent of minor supply rail fluctuations associated with coil movement in the wireless inductive telemetry link.

As mentioned in [83], the threshold voltage of M_1 is subject to vary with temperature. Accordingly, a thermal sensitivity analysis of the prototype IC is summarized in Section 4.6.2.2. However, this is not expected to be problematic since the IC's temperature swing must be limited in order to be biocompatible with implantation in tissue [122], [123]. The ability to achieve a desired reference current using this type of bias circuit lies in precisely fabricating the resistance, R_{bias} , which may vary under the influence of process variation by 20%. In [83], "trimming" by focused ion beam or laser was offered as a solution to this. An alternate solution involves extending the bias circuit to be externally tunable.

Furthermore, several alternatives exist to the bootstrap bias circuit of Figure 4.7. Zener diodes with fixed, known breakdown voltage in the reversed biased regime could be used except that the breakdown voltage is typically outside the supply rails in modern processes [116]. Differences in threshold voltage among enhancement and depletion mode FETs could provide basis for a bias except that depletion FETs are unavailable in mainstream processes [116]. A bandgap reference is another alternative which also provides immunity to power supply variation and to changes in temperature. However, as mentioned, the stimulator IC cannot be allowed to vary much in temperature since it is intended for implantation in biological tissue.

The proposed extension to the bias circuit from the prior generation *Retina-3.5* stimulator IC design [32], [83], of integrating an externally programmable resistance is attractive since a digital communication protocol is already in place to specify stimulus parameters to the implant. It costs little in terms of the protocol to allocate a data word in the configuration packet for digitally tuning the reference current of the bias circuit. This also offers an additional degree of freedom in tuning the stimulus levels to the individual needs of patients. This extension to the core bias circuit is shown in Figure 4.7.

The resistor stack of $R_{bias}^{(5)} - R_{bias}^{(0)}$ forms a digitally selectable resistance based upon the value of the control word (R₅-R₀). This yields a minimum resistance of $R_{bias}^{(base)}$ (when all NFETs in the resistor stack are on) and a maximum resistance of $\left(R_{bias}^{(base)} + \sum_{i=0}^{5} R_{bias}^{(i)}\right)$ (when all the NFETs are off). Through *Hspice* simulation, design values of $R_{bias}^{(base)} = 21.4 \mathrm{k}\Omega$, $R_{bias}^{(5)} = 15.04 \mathrm{k}\Omega$, $R_{bias}^{(4)} = 7.52 \mathrm{k}\Omega$, $R_{bias}^{(3)} = 3.76 \mathrm{k}\Omega$,



Figure 4.7: Tunable biasing circuit for the *multi-bias* generator

 $R_{bias}^{(2)} = 1.88 \mathrm{k}\Omega$, $R_{bias}^{(1)} = 940\Omega$, and $R_{bias}^{(0)} = 470\Omega$ were chosen to yield a value of $20\mu\mathrm{A}$ with approximately $\pm 10\mu\mathrm{A}$ of digital tunability. With $30 \times$ scaling in the output stage of the biphasic amplifier, a $20\mu\mathrm{A}$ reference current should produce a current magnitude of $600\mu\mathrm{A}$ according to the design specification for *Retina-3* and *Retina-3.5*. The NFETs controlled by (R₅-R₀) are sized to give a low impedance path around the bias resistors, effectively shorting them. An additional control bit labeled R_E allows an external off-chip resistance to be connected into the bootstrap reference circuit instead of the programmable resistance stack. The remaining portion of the tunable bias circuit forms $V_{pcasc(Vdd)}$, the cascode bias potential for the PMOS

mirrors of the biphasic output current amplifier, $V_{pcasc(Vcc)}$, the cascode bias potential for the PMOS mirrors in the *multi-bias* generator and stimulus DACs, and V_{ncasc} and V_{nsrc} , the cascode and current source bias potentials for the NMOS mirrors of the gain prescalar and *multi-bias* generator. The on-chip bias resistors are implemented in polysilicon in AMI-1.2 μ m CMOS for the prototype chip, with an implementation area of 185μ m×390 μ m. However, a superior analog process such as AMI-0.5 μ m CMOS with the additional layer for resistor implementation should provide notable reduction in circuit area for the bias circuit based on this tuning technique.

4.4.5 Gain/offset scaling of stimulus currents

A further improvement to the *Retina-3* design concerns the optimization of stimulus current based on the extent of retinal degradation which varies from patient to patient. Generally, more advanced degradation is accompanied by a greater stimulation threshold and thus higher stimulus currents to elicit perception. Moreover, brightness perception is expected to saturate at some current amplitude such that greater currents elicit no further change in perception. This concept is depicted graphically in Figure 4.8 for current amplitude versus DAC digital input at 8-bit DAC resolution.



Figure 4.8: Gain/DC offset concept for optimally tuning the stimulus DAC's output range

The specification for the existing IC designs [32], [83] calls for a 0μ A to 600μ A stimulus current range [41]. The upper current limit is is selectable among 200μ A, 400μ A, or 600μ A levels to provide some flexibility in tuning to match with the patient. The technique proposed here improves upon this by providing some variability in the lower current limit as well. Thus, the effective resolution of the stimulus DAC (8-bits in this prototype chip; 4-bits in *Retina-3.55*) can be optimized to operate over the current range of $i_{threshold}$ to $i_{saturation}$ as defined in Figure 4.8, This prevents the loss of stimulus resolution over the range of excitation currents which are effective for eliciting phosphenes. The offset and gain parameters serve to define the $i_{threshold}$ and $i_{saturation}$ current limits and are implemented as described below.

4.4.5.1 Programmable current gain prescalar

The gain prescalar circuit implements the "gain window" defined in Figure 4.8. This circuit allows the master current reference from the tunable bias circuit to be fractionally scaled with 4-bit linear resolution. The form of the circuit is given in Figure 4.9.



Figure 4.9: Digitally programmable 4-bit reference current gain prescalar circuit

A copy of the reference current from the bias circuit is reproduced from biases V_{ncasc} and V_{nsrc} in NFETs M₃ and M₄. This current is passed into the wide swing
cascoded reference branch of M_1 and M_2 . The current is then fractionally mirrored into the binary weighted branches of M_5 - M_{14} , thus implementing a 4-bit conventional wide swing cascoded current-mode DAC. Since M_{15} and M_{16} form a diode connected load, the voltage at the drain of M_{15} does not rise as strongly as the voltage at the drain of M_3 . The increased V_{ds} across the prescalar DAC (M_5 - M_{14}) leads to a fullscale current (G_3 - G_0 =1111), which is larger than the reference current in M_1 and M_2 . This was overcome by widening M_1 and M_2 to 17× instead of 16×.

The complementary switches controlled by G_3 - G_0 enable the DAC branches by switching the gate potential of the current source PFETs (M_7 , M_9 , M_{11} , and M_{13}) to either the bias voltage from the reference branch (ON state) or to V_{cc} (OFF state). The unswitched branch of M_5 and M_6 prevents a gain of zero such that G_3 - G_0 =0000 does not yield zero current. Selected current from the prescalar DAC is passed info the NFETs M_{15} and M_{16} and is subsequently mirrored into the *multi-bias* generator to supply bias potentials for the stimulus DACs. Therefore, the prescalar current programmed by G_3 - G_0 establishes a full-scale current over which the *multi-bias* DAC exercises 8-bit resolution using bits D_7 - D_0 .

4.4.5.2 Programmable *multi-bias* DC offset DAC

The DC current offset DAC implements the "offset level" (static shift) defined in Figure 4.8. This circuit implements a 4-bit current mode DAC which again fractionally scales the reference current of the tunable bias circuit from 0μ A up to its nominal value of 20μ A. The form of the circuit is shown in Figure 4.10.

The offset DAC is implemented using the proposed *multi-bias* concept in order to reduce area and thus taps gate bias voltages from the central *multi-bias* generator (see Section 4.4.6). The DAC is implemented with the eight PFETs M₁-M₈ equally sized at $\frac{W}{L} = \frac{7.2\mu \text{m}}{4.8\mu \text{m}}$, which implement wide swing cascoded current mirrors in the same manner as in the *multi-bias* stimulus DAC. Again, this does not reflect a need



Figure 4.10: Digitally programmable 4-bit *multi-bias* DC offset DAC (in parallel with the 8-bit *multi-bias* stimulus DAC)

for reduced compliance voltage afforded from the wide swing approach, but rather provides higher output impedance than the simple current mirrors without a heavy routing penalty from additional bias voltages. The cascode PFETs M_5 - M_8 tap the bias potential $V_{pcasc(Vcc)}$ from the tunable bias circuit , which is also used in the *multi-bias* stimulus DAC.

As with the prescalar, the complementary switches controlled by O_3-O_0 enable the DAC branches by routing the gate potential of current source PFETs (M₁-M₄) M₃, M₇, and M₉) to either their associated bias voltage, V_{Obias3} , V_{Obias2} , V_{Obias1} , and V_{Obias0} , from the *multi-bias* generator (ON state) or to V_{cc} (OFF state). The current, i_{offset} , from this DAC is then wired in parallel with the current, i_{DAC} , from the 8-bit stimulus DAC (see Section 4.4.2), as in Figure 4.10 thereby summing the two current outputs.

Due to the nature in which the gain prescalar and the DC offset DAC circuits are implemented, the current gain is a globally programmed setting and is implemented once on the IC. However, the DC offset DAC represents a locally programmable setting. Therefore, in the context of an implantable stimulator containing a array of stimulus circuits, the programmed current gain would apply to all drivers in the array, while independent DC offset DACs would placed in each stimulus circuit.

4.4.6 *Multi-bias* generator

The multi-bias generator, shown in Figure 4.11, is a centrally located circuit which produces gate bias potentials for the 8-bit multi-bias stimulus DACs and the 4-bit DC offset DACs. This is accomplished with conventional binary weighted current mode DACs for bias generation on behalf of the stimulus DACs and offset DACs. The circuit is partitioned into two sections. The upper circuit provides the eight current source bias potentials, V_{Dbias7} , V_{Dbias6} ,..., V_{Dbias0} , for the current source PFETs of the 8-bit multi-bias stimulus DACs. A ninth potential, $V_{pcasc(Vcc)}$, from the tunable bias circuit is also used and is associated with the cascode bias of PFETs M₉-M₁₆.

NFETs M_{17} - M_{24} and M_{25} - M_{32} form a wide swing cascoded binary weighted DAC which fractionally scales the reference current taken from the gain prescalar of Figure 4.9. Recall that the globally programmed gain setting G_3 - G_0 , specifies a scaled copy of the tunable bias circuit's master reference current in NFETs M_{15} and M_{16} of Figure 4.9. This scaled current becomes the reference for the upper section of the bias generator of Figure 4.11 using bias potentials V_{ncasc} and V_{nsrc2} .

NFETs $M_{17}-M_{24}$ and $M_{25}-M_{32}$ mirror this prescaled reference current into binary weighted fractional increments in the same manner as an 8-bit conventional current mode DAC would. These weighted currents are passed into the wide swing cascoded reference branches of M_1-M_8 and M_9-M_{16} , which are equally sized at $\frac{W}{L} = \frac{7.2\mu m}{4.8\mu m}$ in keeping with the *multi-bias* concept for DAC size reduction. The current source bias potentials, V_{Dbias7} , V_{Dbias6} ,..., V_{Dbias0} , along with the cascode bias, $V_{pcasc(Vcc)}$, form the



Figure 4.11: Wide swing cascoded, 8-bit *multi-bias* generator

set of biases which are distributed to the 8-bit *multi-bias* stimulus DACs. With the gain prescalar programmed to its maximum setting, G_3 - G_0 =1111, this configuration allows the nominal 20µA master reference current from the bias circuit to be reproduced in the *multi-bias* DACs with a resolution of 8-bits. This resolution would also be maintained for prescalar settings of G_3 - G_0 <1111, thereby yielding full-scale current in the *multi-bias* DACs of less than 20µA.

A similar arrangement is employed in the lower circuit of Figure 4.11 on behalf of the 4-bit *multi-bias* DC offset DAC which is coupled to the stimulus DAC as in Figure 4.10. This circuit provides four additional current source biases, V_{Obias3} , V_{Obias2} , V_{Obias1} , and V_{Obias0} , but shares the cascode bias potential, $V_{pcasc(Vcc)}$, with the upper circuit.

As before, NFETs M_{41} - M_{48} form a wide swing cascoded binary weighted DAC to fractionally scale the reference current. But since gain prescaling is applied only to the stimulus DAC and not to the DC offset DAC, this reference current is taken from the bias circuit directly instead of from the gain prescalar. Therefore, V_{nsrc} is used here instead of V_{nsrc2} . In the same manner as in the upper circuit, this arrangement is used to produce V_{Obias3} , V_{Obias2} , V_{Obias1} , and V_{Obias0} which, along with $V_{pcasc(Vcc)}$, form the set of biases which are distributed to the 4-bit multi-bias DC offset DACs in the stimulus circuits. This configuration allows the 20μ A reference current from the bias circuit to reproduced in the offset DAC with a 4-bit resolution.

The multi-bias generator accounts for a large amount of chip area owing to the 510 NFET count among the branches of M_{17} - M_{32} and the 30 NFET count among the branches of M_{41} - M_{48} . The 8-bit multi-bias generator of Figure 4.11 occupies an area of 785μ m× 225μ m=0.177mm² in the prototype IC. However, this circuit is implemented only once among a stimulus driver array which may include over 100 driver circuits. The conventional binary weighted DAC contained within the multi-bias generator occupies an area of 595μ m× 180μ m=0.107mm², or 61% of the total multi-bias generator area. The 8-bit stimulus DAC based on the multi-bias concept occupies an area of 220μ m× 120μ m=0.0264mm², or approximately 25% of the area of the conventional 8-bit binary weight DAC. The accumulated area savings in stimulus DACs across the entire driver array justifies the larger multi-bias generator. A driver circuit composed of the 8-bit multibias DAC + biphasic amplifier occupies an area of 0.0558mm² (excluding the DC offset DACs). By comparison, a driver circuit from the Retina-3.5 IC occupies 0.117mm² (excluding the shift and hold data registers).

In an equal area, this would yield approximately twice as many drivers based on the *multi-bias* implementation.

4.5 Simulated and Measured results

4.5.1 *Multi-bias* stimulus DAC

Hspice simulations were performed to test the viability of the *muti-bias* DAC concept. The *multi-bias* DAC and *multi-bias* generator of Figure 4.3a and Figure 4.3b, respectively, based on simple current mirrors is first considered. Due to finite slope in the saturation region of the FET I-V characteristic owing to channel length modulation, there are differences in V_{ds} among the FETs of the current mirror which lead to slightly higher mirrored currents in the *multi-bias* DAC than occur in the reference branches of the *multi-bias* generator (discussed in Section 4.4.6). Each branch of the DAC experiences positive current offsets from the desired current. In a DAC of this structure operated in a binary switched mode, these current offsets accummulate in accordance with the number of branches which are switched on and manifest themselves as non-monotonicities in the DAC transfer characteristic as the digital input is stepped from 00(hex) to FF(hex) (for 8-bit resolution). This is shown in Figure 4.12 and summarized in Table 4.2. The cumulative effect of these current offsets yields DNL and non-monotonicities which become increasingly severe as each DAC input bit D_k switches from logic-0 to logic-1 while bits D_{k-1} to D_0 simulataneously switch from logic-1 to logic-0.

As mentioned in Section 4.4.2, a solution to this involves increasing the output impedance of the current mirrors which exist between the *multi-bias* generator and the *multi-bias* DACs. Therefore, the performance of the wide swing cascode *multi-bias* DAC from Figure 4.5 coupled to the bias generator in Figure 4.11 is now considered.

Figure 4.13 provides a plot of the simulated results of the current of the 8-bit



Figure 4.12: Transfer characteristic for the 8-bit *multi-bias* DAC based on simple current mirrors (simulated)

multi-bias DAC of Figure 4.5 as the digital input is swept from 00(hex) to FF(hex), with the branch current values summarized in Table 4.2. Note that the higher output impedance lowers the severity of the non-monotonicity in the DAC characteristic. In order to further decrease this effect in the prototype chip, the widths of PFETs M_2 and M_{10} corresponding to bit-6 are doubled. The widths of PFETs M_1 and M_9 are quadrupled. This further lowers the non-monotonicity, but begins to erode the elegance of the multi-bias DAC concept as a means to lower DAC implementation area using fixed sized FETs.

4.5.2 Biphasic current output amplifier

Figure 4.14 provides a plot of stimulation current delivered to the load (tissue) impedance of $R_{LOAD} = 10 \mathrm{k}\Omega$, which is measured experimentally as a function of



Figure 4.13: Transfer characteristic for the 8-bit *multi-bias* DAC based on wide swing cascode current mirrors (simulated)

 V_{dd} and V_{ss} varied simultaneously from from 5v to 7v. Thus, the supply drop across the biphasic current amplifier of Figure 4.6 varies from 10v to 14v. Two insights are evident from this data. The stimulation current is much more dependent on the supply rails than would be desireable. This occurs from a layout mistake in which the bias circuit of Figure 4.7 was wired to operated from V_{dd} to V_{ss} instead of V_{cc} to V_{ss} , thus accounting for upwards of twice the intended supply drop across the tunable bias circuit. This has the effect of modulating the master reference current with the supply rails.

A second insight from this data is that the matching between the amplitudes of the anodic and cathodic pulses becomes worse with increasing voltage drop between V_{dd} and V_{ss} . Although acceptable at $V_{dd}/V_{ss}=\pm5v$, the matching is quite poor at $V_{dd}/V_{ss}=\pm7v$. This is the same problem which occurred in the biphasic output stage



Figure 4.14: Stimulus current dependence on supply variation (experimentally measured at the output of the biphasic current amplifier)

of Figure 3.10 in the *Retina-3.55* stimulator IC design.

Since the circuit is Figure 4.6 is of a similar structure to that of Figure 3.10 in the *Retina-3.55* stimulator IC, the same impact ionization occurs leading to current amplitude mismatch. To re-itereate, the cause of the large mismatch is actually a higher anodic current than should occur with respect to the cathodic current, owing to impact ionization in the FETs due to high V_{ds} . In Figure 4.6, M₃ and M₄ are wide swing connected and the gate of M₅ is connected to a constant potential, V_{ncasc} . Thus, the voltage appearing at V_{ds} of M₅ is $V_{dd} - V_{ss} - (V_{ncasc} - V_{gs5}) - |V_{gs3}|$ and hence any increase in V_{dd}/V_{ss} directly increments V_{ds} of M₅. High V_{ds} in a transistor results in high electric field in the channel, which imparts excessive energy to the channel electrons especially near the drain region. These high energy electrons generate electron-hole pairs due to impact ionization. The holes are attracted to the negatively biased bulk where they appear as a substrate current. The associated electrons from the electron-hole pairs increase the drain current in M_5 [110]. This excessive drain current tracks in M_3 and M_4 and is reflected in the anodic current. A proposed solution to correct this in Figure 4.6 for the *multi-bias* prototype chip is similar to the method suggested for the *Retina-3.55* IC design and is again discussed in Section 4.6.3.

4.5.3 Tunable bias circuit

The tunable bias circuit of Figure 4.7 is designed to produce a nominal reference current of 20μ A for the gain prescalar and *multi-bias* generator. Recall that since AMI-1.2 μ m CMOS provides no special "high-resistance" layer, the circuit's resistance stack was implemented in polysilicon. With a tolerance of $\pm 20\%$ expected, circuit simulations were performed to confirm that 20μ A was achievable across this tolerance range. Results are provided in Figure 4.15.

The reference current is plotted against the digital selector word for the resistance stack, which is tunable using configuration bits (R_5 - R_0). The available current range is plotted for nominal resistance values and for $\pm 10\%$, $\pm 20\%$, $\pm 30\%$ deviation from nominal. These simulations indicate that the targeted 20μ A lies within the programmable resistance range for tolerances out to $\pm 30\%$. These curves also manifest integral non-linearity across the full resistance range as well as differential non-linearity in the size of the resistance step change (differential non-linearity). This is a consequence of intersecting a linear I-V characteristic (resistance) with a quadratic one (NFET M₁ in Figure 4.7). These non-linearities do not represent a serious problem, since the goal of this arrangement is to tune out process variation or to a lesser extent to globally returne the stimulus DAC to operate at higher currents.



Figure 4.15: Amplitude of the reference current versus resistance selector word for variation in tolerance (simulated since bias current is not accessible off-chip)

4.5.4 Programmable current gain prescalar

Figure 4.16 provides experimental measurement of the performance of the gain prescalar of Figure 4.9. Since the biphasic amplifier of Figure 4.6 is exhibiting anodic/cathodic stimulus current mismatch at $V_{dd}/V_{ss} = \pm 7v$, the IC was instead operated at $V_{dd}/V_{ss} = \pm 5v$ where matching is more acceptable. As 600μ A stimulus current into a $10k\Omega$ load is unattainable at $V_{dd}/V_{ss} = \pm 5v$, the tunable bias circuit is recalibrated to produce full-scale stimulation currents of 400μ A in the output stage of the biphasic amplifier.

These measurements were captured using a TEK684B Tektronics oscilloscope which is set to average 100 consecutive signal acquisitions. Sixteen separate measurements were taken associated with the programmable range of the 4-bit prescalar circuit. For each gain setting, the digital input to the multi-bias stimulus DAC is



Figure 4.16: Performance of the 4-bit gain prescalar and 8-bit *multi-bias* stimulus DAC (experimentally measured)

swept from 00(hex) to FF(hex). This produces a stimulus current into the 10k Ω load impedance of Figure 4.6 ranging from 0 μ A to a maximum value established by prescalar current (×30), with a full-scale expected anodic and cathodic current of 400 μ A. These sixteen plots are superimposed in order to evaluate the performance the gain prescalar. The DC offset DAC of Figure 4.10 was set to O₃-O₀=0000 during these measurements. These plots indicate good integral linearity and monotonicity are attainable using the *multi-bias* DAC concept. They also show that the gain prescalar can effectively set an *i_{saturation}* limit for the stimulus circuits as defined in Figure 4.8.

4.5.5 Programmable *multi-bias* DC offset DAC

Figure 4.17 provides experimental measurement of the performance of the 4-bit *multi*bias DC offset DAC of Figure 4.10. As before, the IC is operated at $V_{dd}/V_{ss} = \pm 5v$ to yield phase-matched 400 μ A full-scale stimulation currents.



Figure 4.17: Performance of the 4-bit *multi-bias* DC offset DAC (experimentally measured)

Again, sixteen separate measurements were taken for each selectable offset level of the 4-bit *multi-bias* DC offset DAC. For each offset setting, the digital input to the 8-bit *multi-bias* stimulus DAC is swept from 00(hex) to FF(hex). This yields a stimulation current ranging from a minimum value established by the DC offset DAC (×30) to a maximum value established by the prescalar circuit (×30), with a full-scale expected anodic and cathodic current of 400μ A. The sixteen plots are superimposed on a single plot to yield the characteristic of the DC offset DAC. Note that the gain of the prescalar circuit and the DC level from the offset DAC must be appropriately sized with respect to one another to achieve an operating stimulus current range which does not exceed the output sourcing/sinking capabilities of the biphasic amplifier. At $V_{dd}/V_{ss} = \pm 5v$ load current much beyond 400μ A will force PFETs M₇ and M₈ or NFETs M₉ and M₁₀ of the biphasic amplifier into triode and subsequently clip the output current. This is evident in the curves of Figure 4.17. During these DC offset measurements, the gain prescalar is programmed at a setting of G₃-G₀=1000(binary), corresponding to a full-scale load current of approximately 260μ A. At this level, a DC offset programmed setting near O₃-O₀=0111(binary) and beyond will lead to clipping. However, in practice the gain prescalar and offset DAC would together be programmed to implement $i_{threshold}$ and $i_{saturation}$ current limits within the drive capabilities of the biphasic output current amplifier.

4.5.6 Repeatability

The ability to produce consistent output becomes an issue when implementing an array of stimulator circuits based on the *multi-bias* DAC concept. Due to process variation, deviations from intended FET geometry can arise between corresponding devices of the *multi-bias* generator and *multi-bias* DACs. This introduces an opportunity for performance differences among identical *multi-bias* DAC circuits. The FETs of the *multi-bias* generator and the *multi-bias* DACs were sized at four times minimum length and width as a compromise between process variation and implementation area. To facilitate evaluating performance variation, a number of identical *multi-bias* DAC and biphasic amplifier circuits were implemented which derive common bias potentials from the central *multi-bias* generator. A comparison among three such stimulus circuits is provided in Figure 4.18.

For each circuit, the digital input to the *multi-bias* stimulus DAC is swept from 00(hex) to FF(hex), with the associated DC offset DAC set to zero (O₃-O₀=0000(binary)) and the gain prescalar set to maximum (G₃-G₀=1111(binary)). As before, the circuits are powered at $V_{dd}/V_{ss} = \pm 5v$ with the tunable bias circuit recalibrated to yield $400\mu\text{A}$ full-scale load currents from the biphasic amplifiers. Figure 4.18 indicates that circuit instances #2 and #3 track well but that instance #1 is deviant by an amount approximately 10 LSB step sizes or equivalently 4% of the DAC full swing. This discrepancy begins to occur at the MSB transition halfway through the staircase characteristic. Insights gathered from circuit simulation indicate that the fully cascoded implementation of the *multi-bias* DAC, proposed in Section 4.6.2 as a design enhancement to the wide swing cascoded configuration, will reduce the DNL errors at the major bit transitions and should improve repeatability among duplicate instances of *multi-bias* DAC circuits.



Figure 4.18: Performance repeatability of the *multi-bias* concept (experimentally measured)

4.5.7 Measurement summary and die photo

A summary of the experimental measurements and simulations results is provided in Table 4.1. A die photograph of the *multi-bias* DAC prototype chip is shown in Figure 4.19. The chip was implemented in the AMI-1.2 μ m two metal layer, two polysilicon layer, CMOS process through the MOSIS facility. The die measures 2.2mm×2.2mm. The area occupied on the chip by the 8-bit *multi-bias* generator is 0.177mm², which while appearing significant is incurred only one per chip to service an array of *multi-bias* DACs. The binary weighted DAC employed within the *multi-bias* generator occupies an area of 0.107mm². The *multi-bias* DAC on the other hand consumes 0.0265mm², for a savings of 75% compared with the conventional binary current-weighted DAC, with potentially higher savings from tighter layout in more advanced IC processes having more metal layers for routing the bias potentials.

Technology	MOSIS $1.2\mu m$ CMOS
Die size	$2.2\mathrm{mm}$ $ imes$ $2.2\mathrm{mm}$
Area	
<i>multi-bias</i> generator	$0.177 \mathrm{mm}^2$
multi-bias DAC	0.0264 mm ²
conventional binary	
current-weighted DAC	$0.107 \mathrm{mm}^2$
biphasic amplifier	$0.0237 \mathrm{~mm^2}$
Amplitude resolution	8-bits
Anodic current INL	-3.11
Cathodic current INL	1.59
Anodic current DNL	2.15
Cathodic current DNL	2.11
Anodic/Cathodic mismatching	14.56 LSB (5.74%)
Supply sensitivity	$2.5 \frac{\mu A}{V}$

 Table 4.1: Chip performance specification and measurements



Figure 4.19: Die micrograph of the multi-bias DAC prototype IC $\,$

4.6 Design enhancements

4.6.1 Noise immunity on the bias voltages

A potential limitation to good performance in using the *multi-bias* cencept to reduce area concerns the negative impact of noise on the bias voltages. Future implant ICs will contain arrays of hundreds of stimulator circuits or more, with the bias potentials for the *multi-bias* DACs distributed across the chip from a central *multibias* generator. In this context there are at least two foreseeable sources of corrupting noise.

The stimulator IC designs reported in [32], [83], and [101], represent a mixed signal environment with clocked fifos providing digital data to analog stimulus circuits. Digital signals such as the clock and latch-enables will be distributed throughout the chip along with the analog DC bias potentials for the *multi-bias* stimulus DACs. Therefore, there is ample opportunity for noise from digital signals on adjacent interconnect to capacitively couple onto the bias interconnect and on to power rails supplying the analog circuits. In the AMI-1.2 μ m process with its two metal layers, there are very limited resources to protect the bias potentials from noise on adjacent interconnect and from noise injected into the substrate without compromising routability. However, in more modern processes providing five to seven metal layers, it should be straight forward to gather all of the DC bias potentials into a tight common group with grounded interconnect of either side of the group and grounded metal shield planes above and below the group. Since the bias potentials are DC there is no concern that they will impart capacitively coupled noise to one another. However, clock feedthrough noise may be imposed onto the biases from the DAC circuitry, as discussed below.

When the complementary switches in the *multi-bias* DACs are toggled, the associated clock feedthrough can introduce noise onto the bias interconnect which can adversely affect other *multi-bias* DACs which share those biases. This arrangement is shown in Figure 4.20a taken from Figure 4.5. PFET M_2 implements a pullup of the gate of M_3 to V_{dd} inorder to disengage the branch current i_{DAC} , whereas M_1 engages the branch current by routing the *current source bias* to M_3 . During this time M_1 can introduce capacitively coupling noise onto the *current source bias*. When considering that this bias voltage feeds every stimulus DAC throughout an array of DACs with potentially independent switching times, the noise consequences could become significant.



Figure 4.20: Clock feedthrough in engaging current branches of the multi-bias DAC

Figure 4.20b offers an alternative to this arrangement for engaging/disengaging the branch current using a switch in series with i_{DAC} . This frees the bias potential to be routed directly to the gate of M₅ as with the cascode transistor M₆. This moves the clock feedthrough problem away from the gate, but re-introduces it into the DAC's output at the drain of M₇. The associated noise at M₇ would be confined to this DAC and should not affect other DACs in an array structure. Furthermore, as it relates to electrical stimulation in the retinal prosthesis, the time scale of this switching noise is much shorter than the stimulus pulse widths needed for ganglion cell excitation [17], [18], and of the refractory times of the neurons/cells [124]. Therefore, this transient switching noise would not be expected to elicit perceptual artifacts. Moreover, moving the digital switches away from the gate of M_3 introduces the added benefit that the bias potential is "buffered" by the cummulative gate capacitance of PFETs M_3 and M_4 for each DAC throughout the driver array, thereby providing additional noise immunity. The tradeoff with the arrangement of Figure 4.20b is that additional supply voltage "headroom", or compliance, is required to keep M_5 and M_6 out of the linear region, thereby necessitating higher V_{cc} with an accompanying increase in power dissipation.

4.6.2 Improvements to non-monotonicity in the *multi-bias* DAC

An improvement in DNL at the major bit transitions and in INL for the digital input to analog output transfer characteristic is achieved by replacing the wide swing cascode mirrors in the DAC with fully cascoded mirrors. This is shown in Figure 4.21 and Figure 4.22 for the *multi-bias* generator and the *multi-bias* DAC, respectively. These provide greater output impedance than their wide swing counterparts since the FETs operate deeper in saturation. This comes at the expense of a greater number of bias potentials which must be distributed to the DACs (eight current source biases plus eight cascode biases, for a total of 16 per DAC for 8-bit resolution).



Figure 4.21: Fully cascoded, 8-bit *multi-bias* generator



Figure 4.22: Fully cascoded, 8-bit *multi-bias* bias DAC

The accompanying improvement in linearity of the *multi-bias* DAC transfer characteristic is evident from Figure 4.23. A fully cascoded arrangement for the *multi-bias* DAC and the *multi-bias* bias generator yields a staircase with no non-monotonicity throughout the full range of the 8-bit digital input. The DAC suffers a slight distortion at the major bit transitions, where a current source for bit_n engages and the current sources for bit_{n-1} - bit_0 disengage. But, this is significantly reduced when compared to wide swing cascode mirrors. The sudden drops in adjacent peak amplitudes in the sawtooth waveform of Figure 4.23b represent the DNL error in the transfer characteristic. The worst case DNL picture here is estimated at 0.8 LSB as indicated in Figure 4.23b at the digital input code, D_7 - $D_0=80$ (hex), or 128(dec) and as shown in the inset of Figure 4.23a at the MSB low to high transition (bit-7). The DNL statistics for *multi-bias* DACs based on simple current mirrors, wide swing cascode current mirrors and fully cascoded current mirrors is summarized in Table 4.2. The trend in the average value of the sawtooth waveform as a function of the DAC digital input code represents the INL error in the transfer characteristic. Worst case INL is under 1 LSB for all digital input codes.



Figure 4.23: Digital input to analog output transfer characteristic of the fully cascoded, 8-bit *multi-bias* bias DAC (simulated since the prototype chip does not contain the fully cascoded configuration)

4.6.2.1 Sensitivity of bias voltages to noise

A sensitivity analysis of multi-bias DAC branch currents to bias noise is summarized in Table 4.3. These branch currents correspond to i_7-i_0 as annotated on the fully cascoded multi-bias DAC of Figure 4.22. In this study, the branch currents were simulated with ±10mv of DC noise offset from the nominal values of the eight current source bias potentials, $V_{DbiasS7}-V_{DbiasS0}$ of PFETs M₁-M₈, and the eight cascode bias potentials, $V_{DbiasC7}-V_{DbiasC0}$ of PFETs M₉-M₁₆.

As expected, the noise on biases $V_{DbiasS7}-V_{DbiasS0}$ imparted greater branch current deviations than the biases $V_{DbiasC7}-V_{DbiasC0}$. Furthermore, the lower significant bits exhibit more sensitivity expressed in percent difference, which will more noticeably affect the transfer characteristic owing to the more frequent bit transitions in the digital input. However, as the nominal currents increase by factors of two for each successive significant bit, the absolute deviation from ±10mv of bias noise imparts a

DAC code bit #	$\begin{array}{c} \text{desired} \\ \text{current} \\ (^1) \end{array}$	deviation in the simple current mirror $topology^2$			deviation in the wide swing topology ³		deviation in the fully cadcoded topology ⁴			
	()	actual	% diff.	DNL^5	actual	% diff.	DNL^5	actual	% diff.	DNL^5
		current	w.r.t.		current	w.r.t.		current	w.r.t.	
			desired			desired			desired	
			current			current			current	
7	10.039	12.973	29.22~%	-58.9398	10.164	1.24~%	-12.725	10.081	0.42~%	-0.8011
6	5.0196	7.3093	45.62~%	-43.5378	5.2243	4.08 %	-9.1753	5.0547	0.70~%	-0.5130
5	2.5098	4.2629	$69.85 \ \%$	-30.9536	2.7341	8.94~%	-6.1051	2.5361	1.05~%	-0.3217
4	1.2549	2.5996	107.16~%	-20.6732	1.4607	16.40~%	-3.7349	1.2740	1.52~%	-0.1853
3	0.6275	1.6773	167.32~%	-11.9981	0.8018	27.79~%	-1.9218	0.6412	2.19~%	-0.0846
2	0.3137	1.1508	266.82~%	-4.5687	0.4544	44.84~%	-0.5627	0.3235	3.12~%	-0.0132
1	0.1569	0.8310	429.76~%	1.6979	0.2645	68.62~%	0.3859	0.1635	4.23~%	0.0305
0	0.0784	0.6194	689.74~%	6.8973	0.1558	98.65~%	0.9865	0.0827	5.42~%	0.0542

 Table 4.2: Branch current deviations leading to DAC DNL

¹Derived from the ideal transfer characteristic of an 8-bit DAC at ned to a full-scale range of 20μ A. ²Computed from the simulated data plotted in Figure 4.12.

³Computed from the simulated data plotted in Figure 4.13.

⁴Computed from the simulated data plotted in Figure 4.23a.

⁵Differential nonlinearity is defined as $\left(\frac{i_{(2^n+1)}-i_{(2^n)}}{\Delta i_{LSB(ideal)}}-1\right)$, where $i_{(2^n)}$ is DAC current corresponding

to dac digital input 2^n , for bit-n. Therefore, DNL>0 indicates a monotonic step greater than 1-LSB of the ideal transfer characteristic, $-1 < \text{DNL} \le 0$ represents a monotonic step less than 1-LSB, and DNL ≤ -1 implies a non-monotonic (negative) step.

bias ¹	nominal	nominal	$\Delta i_{DS}{}^3$ from	% diff	$\Delta i_{DS}{}^3$ from	% diff
	value	i_{DS}^2	$+10 \mathrm{mV} \ \Delta \mathrm{V}$		$-10 \mathrm{mV} \ \Delta \mathrm{V}$	
	$[V_{DC}]$	$[\mu A]$	[nA]		[nA]	
$V_{DbiasS7}$	5.188	10.030	-189.43	-1.89	191.00	1.90
$V_{DbiasS6}$	5.473	5.0270	-138.39	-2.75	140.12	2.79
$V_{DbiasS5}$	5.67	2.5220	-100.19	-3.97	102.06	4.05
$V_{DbiasS4}$	5.806	1.2670	-72.56	-5.72	74.50	5.88
$V_{DbiasS3}$	5.9	0.6379	-52.76	-8.28	54.82	8.60
$V_{DbiasS2}$	5.965	0.3219	-37.57	-11.73	39.94	12.47
$V_{DbiasS1}$	6.011	0.1628	-25.28	-15.61	27.91	17.24
$V_{DbiasS0}$	6.046	0.0823	-15.78	-19.25	18.28	22.30
$V_{DbiasC7}$	3.037	10.030	-5.70	-0.06	5.70	0.06
$V_{DbiasC6}$	3.653	5.0270	-3.86	-0.08	3.84	0.08
$V_{DbiasC5}$	4.078	2.5220	-2.62	-0.10	2.61	0.10
$V_{DbiasC4}$	4.373	1.2670	-1.81	-0.14	1.81	0.14
$V_{DbiasC3}$	4.576	0.6379	-1.27	-0.20	1.27	0.20
$V_{DbiasC2}$	4.716	0.3219	-0.89	-0.28	0.89	0.28
$V_{DbiasC1}$	4.816	0.1628	-0.60	-0.37	0.60	0.37
$V_{DbiasC0}$	4.893	0.0823	-0.38	-0.46	0.38	0.46

Table 4.3: Branch current sensitivity to bias noise

¹Bias potentials are in reference to the 8-bit fully cascoded *multi-bias* generator of Figure 4.21 biased to produced 20μ A full-scale current in the *multi-bias* DAC of Figure 4.22 ("S" subscript refers to a current source bias potential; "C" subscript refers to a cascode bias potential). ²Branch current is taken in association with the corresponding bias. ³Bias potential is offset ±10mV to model noise. correspondingly greater absolute deviations in the nominal current value. If routing resources allow, an ideal solution would provide grounded shielding for all sixteen bias potentials. If a compromise must be made, then shielding preference should be given to the current source biases, $V_{DbiasS7}-V_{DbiasS0}$, owing to their greater sensitivity to noise.

4.6.2.2 Thermal sensitivity of the Multi-bias DAC

Figure 4.24 provides insight into the temperature sensitivity of the current outputs of the 8-bit *multi-bias* DAC and the biphasic current amplifier. For this simulation, the DAC is retuned to produce 20μ A at 37°C associated with human body temperature in the context of implantation.



Figure 4.24: Thermal dependence of currents from the *multi-bias* DAC and the biphasic current amplifier (simulated due to the difficulty to experimentally control chip temperature precisely)

The curves of Figure 4.24 consider a coverage of $\pm 10^{\circ}$ C around a nominal body temperature of 37°C. The current output from the *multi-bias* DAC exhibits a nearly

linear dependence with a thermal coefficient of $-0.0249 \frac{\mu A}{\circ C}$, over the range of 27°C– 47°C. The anodic stimulus current from the biphasic amplifier exhibits a thermal slope of $0.5421 \frac{\mu A}{\circ C}$, over the same range, while the cathodic current manifests a slope of $0.7154 \frac{\mu A}{\circ C}$. The greater slope for the cathodic current indicates that the NMOS current mirrors in the biphasic amplifier are more sensitive to temperature variation than the PMOS mirrors. Furthermore, this implies that current amplitude mismatch will become gradually worse for elevated temperature. This is indicated by the dashed curve (cathodic current magnitude) in comparison to the anodic current in Figure 4.24. However, this is not expected to become a problem since the IC when implanted must remain close to body temperature in order to be biocompatible. Numerical, iterative, thermal simulations [125], [126] suggest an intraocular temperature increase of approximately 0.4° C- 0.6° C in the chip positioned at mid-vitreous and approximately 0.2° C at the retina surface, due to power dissipation in the sixty channel *Retina-3.5* stimulator IC implanted in an anatomically derived 0.25mm 2D head/eye model.

4.6.3 Improvements to the biphasic amplifier output stage

The proposed solution to remedy the amplitude mismatch in the anodic/cathodic currents at $V_{dd}/V_{ss}=\pm7v$ from the output stage of Figure 4.6 is the same as that proposed for the circuit of Figure 3.10 in the *Retina-3.55* stimulator IC. Specifically, the associated impact ionization due to the high V_{ds} in M₅ can be eliminated by introducing a number of diode-connected NFETs between M₄ and M₅ to absorb some of the voltage drop. As was the case in the circuit of Figure 3.10, and also in the circuit of Figure 4.6, this will not increase power dissipation since the voltage across and current through the transistor stack is unchanged.

4.7 Summary

A novel modification to the conventional binary-weighted current-mode DAC based on distributed multiple bias potentials has been presented for use in bio-implantable neuro-stimulators. This new approach significantly decreases the implementation area when compared to the conventional DAC structure. Transistor counts are reduced from $2(2^N - 1)$ FETs for an N-bit conventional binary-weighted DAC using cascoded mirrors to 2N FETs for the reduced area *multi-bias* DAC. Die area savings for an 8-bit DAC are approximately 52%, with possible higher savings with tighter layout afforded by newer IC processes with more metal layers. The benefits of reduced area should prove beneficial for increasing spatial resolution in micro-stimulators and consequently the effectiveness of visual prostheses. Current gain prescalar and DC offset DAC circuits were also introduced to optimize the effective stimulus current range for the needs of individual patients. These improvements to the existing IC designs were implemented in a 2.2mm prototype IC in AMI-1.2 μ m CMOS.

Chapter 5

Intraocular electromagnetic and thermal modeling

5.1 Introduction

As with all implantable electronic devices, the operation of the retinal prosthesis implanted in a human patient is expected to bring about an increase in the natural steady state temperature of the eye and surrounding head tissues. Therefore, a study is undertaken using numerical simulation to predict the extent of temperature increase due to the operation of the retinal prosthesis. Ocular heating is accounted for by inductive telemetry with the implant for wireless power and data transfer (for which the specific absorption rate of electromagnetic power deposition is quantified) and the power dissipation in the implantable retinal stimulator microchip positioned at midvitreous. Although the prosthesis will eventually consist of additional components including the receiving coil and mechanical support structures, these thermal studies are limited at this time to the SAR associated with inductive coupling and the power consumption in the implantable microchip itself.

In recent years, studies and results have been reported in which the temperature increases in the head are of interest. Many of these have been brought about from the proliferation of cellular phones and concerns of their influence on the human head [127]–[129]. Furthermore, supposed links between electromagnetic exposure and the formation of cataracts [130], [131] has led to increased interest in studies of thermal heating in the human eye due to radiation in wireless computer networks [122], from infrared radiation in industrial settings [132], and to forms of electromagnetic exposure [133]. These studies have been primarily conducted at frequencies in the vicinity of 700Mhz to 2.45Ghz, due to the proliferation of wireless devices operating in these bands.

In this chapter, the methods and models are described which are used to compute estimates of heating in the human eye and surrounding head tissues subjected to the operation of the epi-retinal prosthesis. Electromagnetic power deposition resulting from inductive telemetry and power dissipation from the implantable stimulator IC are the heating mechanisms which are characterized.

5.2 Methods

Two numerical methods have been implemented to characterize the thermal behavior of the retinal prosthesis. Specific absorption rate of electromagnetic exposure associated with inductively coupling to the implant (for power and data telemetry) introduces heating in the ocular tissues. The first method introduced in Section 5.2.1, referred to as the numerical FDTD method, computes the steady state electric and magnetic field distribution in the 2D head/eye model. Subsequently, the specific absorption rate is computed from the $\vec{\mathbf{E}}$ -field distribution into order to characterize the power deposition in the biological tissues corresponding to this exposure. The second method introduced in Section 5.2.2, referred to as the numerical thermal method, computes an estimate of temperature elevation above normal due to the electromagnetic power deposition characterized by specific absorption rate and from an estimate of the retinal stimulator IC's power dissipation. The mathematical development of these two methods will be briefly introduced.

5.2.1 Finite difference time domain simulation of Maxwell's equations

Numerical estimation of the specific absorption rate for the irradiated biological tissues derives from Maxwell's equations which fully characterize the electromagnetic process in the time domain. There are several popular approaches to numerical electromagnetics [134]. For the work presented here, the well-developed *Finite Difference Time Domain* (FDTD) method is utilized with special extension to address waveenergy absorption at the model-boundary. This methodology allows for a modelindependent implementation in which wave propagation can be simulated with absorption at the model boundary taken into account. Section 5.2.1.1 reviews the discretization of Maxwell's equations in space and time for implementation in keeping with the FDTD method. Section 5.2.1.2 briefly introduces the absorbing boundary conditions which have been integrally developed into the classical FDTD.

5.2.1.1 Space/time discretization of the coupled equations

Maxwell's equations for non-magnetic materials expressed in differential form are given in Equations 5.1–5.2.

$$\frac{\partial \vec{\mathbf{D}}}{\partial t} = \nabla \times \vec{\mathbf{H}} \tag{5.1}$$

$$\frac{\partial \mathbf{H}}{\partial t} = -\frac{1}{\mu_0} \nabla \times \vec{\mathbf{E}}$$
(5.2)

where $\vec{\mathbf{E}}$, $\vec{\mathbf{H}}$, $\vec{\mathbf{D}}$, are three dimensional vectors that represent the electric field, the magnetic field, and electric flux density (or electric induction), respectively. For linear isotropic materials, $\vec{\mathbf{D}}$ and $\vec{\mathbf{E}}$ are simply proportional and related through a complex

dielectric constant, ϵ^* , as given in Equation 5.3.

$$\vec{\mathbf{D}} = \epsilon^* \vec{\mathbf{E}} \tag{5.3}$$

In order to have coupled $\vec{\mathbf{E}}$ and $\vec{\mathbf{H}}$ quantities that are similar in magnitude such that finite–difference based numerical implementations do not accumulate error, a **normalized** representation of Equations 5.1–5.2 is considered. By dividing $\vec{\mathbf{E}}$ by $\sqrt{\frac{\mu_0}{\epsilon_0}}$, Equations 5.1–5.2 can be written as

$$\frac{\partial \vec{\mathbf{D}}}{\partial t} = \frac{1}{\sqrt{\mu_0 \epsilon_0}} \nabla \times \vec{\mathbf{H}}$$
(5.4)

$$\frac{\partial \vec{\mathbf{H}}}{\partial t} = -\frac{1}{\sqrt{\mu_0 \epsilon_0}} \nabla \times \vec{\mathbf{E}}$$
(5.5)

Expanding the cross products of Equations 5.4–5.5 and equating vector components gives the following six coupled equations for the components of vectors $\vec{\mathbf{D}}$ and $\vec{\mathbf{H}}$.

$$\frac{\partial D_x}{\partial t} = \frac{1}{\sqrt{\mu_0 \epsilon_0}} \left(\frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z} \right)$$
(5.6)

$$\frac{\partial D_y}{\partial t} = \frac{1}{\sqrt{\mu_0 \epsilon_0}} \left(\frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x} \right)$$
(5.7)

$$\frac{\partial D_z}{\partial t} = \frac{1}{\sqrt{\mu_0 \epsilon_0}} \left(\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} \right)$$
(5.8)

$$\frac{\partial H_x}{\partial t} = \frac{1}{\sqrt{\mu_0 \epsilon_0}} \left(\frac{\partial E_y}{\partial z} - \frac{\partial E_z}{\partial y} \right)$$
(5.9)

$$\frac{\partial H_y}{\partial t} = \frac{1}{\sqrt{\mu_0 \epsilon_0}} \left(\frac{\partial E_z}{\partial x} - \frac{\partial E_x}{\partial z} \right)$$
(5.10)

$$\frac{\partial H_z}{\partial t} = \frac{1}{\sqrt{\mu_0 \epsilon_0}} \left(\frac{\partial E_x}{\partial y} - \frac{\partial E_y}{\partial x} \right) \tag{5.11}$$

Obviously, the relations of Equations 5.6–5.11 reflect the coupled nature of Maxwell's equations. The finite difference time domain methods which approximate these equations (originally proposed in [135]) assume the availability of $\vec{\mathbf{H}}$ which is then used to compute $\vec{\mathbf{D}}$, using Equations 5.6–5.8. A time domain equation derived from Equation 5.3 is used to compute $\vec{\mathbf{E}}$ from $\vec{\mathbf{D}}$. Subsequently, Equations 5.9–5.11 are used to compute $\vec{\mathbf{H}}$ from $\vec{\mathbf{E}}$, for the following time step, and so forth in a "leap–frog" fashion. However, to implement such an algorithm, the components of $\vec{\mathbf{E}}$ are offset by one-half of a step in space and one-half of a step in time with respect to the components of $\vec{\mathbf{H}}$. This is implemented in accordance with the *Yee Cell* conventions [135] as illustrated in Figure 5.1.

With respect to the discretized indices (i, j, k) for the model axes (where $x = i \, \delta x$, $y = j \, \delta y$, and $z = k \, \delta z$) and the discretized time n (where $t = n \, \delta t$), the components of $\vec{\mathbf{H}}$ are defined along integer time steps, n, for n=0,1,2,..., while the components of $\vec{\mathbf{E}}$ (and $\vec{\mathbf{D}}$) are defined along fractional time steps, $n + \frac{1}{2}$. With regard to spatial dimension, the components of $\vec{\mathbf{H}}$ and $\vec{\mathbf{D}}$ are defined as $D_{x \, (i+\frac{1}{2},j,k)}^{n+\frac{1}{2}}$, $D_{y \, (i,j+\frac{1}{2},k)}^{n+\frac{1}{2}}$, $D_{z \, (i,j,k+\frac{1}{2})}^{n+\frac{1}{2}}$, $H_{x \, (i,j+\frac{1}{2},k+\frac{1}{2})}^{n}$, $H_{y \, (i+\frac{1}{2},j,k+\frac{1}{2})}^{n}$, and $H_{z \, (i+\frac{1}{2},j+\frac{1}{2},k)}^{n}$. By using these conventions for the definition of the vector components of $\vec{\mathbf{E}}$ and $\vec{\mathbf{H}}$, finite difference approximations for the space and time derivatives of Equations 5.6–5.11 can be developed and are given in Equations 5.12–5.29, where δx , δy , and δz are the cell dimensions in the x, y, and z directions, respectively, and δt is the time step.



Figure 5.1: Yee cell conventions for vector assignments for \vec{E} and \vec{H}

$$\frac{\partial D_x}{\partial t} = \frac{D_{x\ (i+\frac{1}{2},j,k)}^{n+\frac{1}{2}} - D_{x\ (i+\frac{1}{2},j,k)}^{n-\frac{1}{2}}}{\delta t} \quad (5.12) \qquad \frac{\partial H_x}{\partial t} = \frac{H_{x\ (i,j+\frac{1}{2},k+\frac{1}{2})}^{n+1} - H_{x\ (i,j+\frac{1}{2},k+\frac{1}{2})}^n}{\delta t} \quad (5.13)$$

$$\frac{\partial D_y}{\partial t} = \frac{D_{y\ (i,j+\frac{1}{2},k)}^{n+\frac{1}{2}} - D_{y\ (i,j+\frac{1}{2},k)}^{n-\frac{1}{2}}}{\delta t} \quad (5.14) \qquad \frac{\partial H_y}{\partial t} = \frac{H_{y\ (i+\frac{1}{2},j,k+\frac{1}{2})}^{n+1} - H_{y\ (i+\frac{1}{2},j,k+\frac{1}{2})}^n}{\delta t} \quad (5.15)$$

$$\frac{\partial D_z}{\partial t} = \frac{D_{z\ (i,j,k+\frac{1}{2})}^{n+\frac{1}{2}} - D_{z\ (i,j,k+\frac{1}{2})}^{n-\frac{1}{2}}}{\delta t} \quad (5.16)$$

$$\frac{\partial H_z}{\partial t} = \frac{H_{z\ (i+\frac{1}{2},j+\frac{1}{2},k)}^{n+1} - H_{z\ (i+\frac{1}{2},j+\frac{1}{2},k)}^n}{\delta t}$$
(5.17)

$$\frac{\partial D_x}{\partial y} = \frac{D_{x\,(i+\frac{1}{2},j+1,k)}^{n+\frac{1}{2}} - D_{x\,(i+\frac{1}{2},j,k)}^{n+\frac{1}{2}}}{\delta y} \qquad \qquad \frac{\partial H_x}{\partial y} = \frac{H_{x\,(i,j+\frac{1}{2},k+\frac{1}{2})}^n - H_{x\,(i,j-\frac{1}{2},k+\frac{1}{2})}^n}{\delta y} \tag{5.19}$$

$$\frac{\partial D_x}{\partial z} = \frac{D_{x\,(i+\frac{1}{2},j,k+1)}^{n+\frac{1}{2}} - D_{x\,(i+\frac{1}{2},j,k)}^{n+\frac{1}{2}}}{\delta z}}{(5.20)} \qquad \frac{\partial H_x}{\partial z} = \frac{H_{x\,(i,j+\frac{1}{2},k+\frac{1}{2})}^n - H_{x\,(i,j+\frac{1}{2},k-\frac{1}{2})}^n}{\delta z}}{(5.21)}$$

$$\frac{\partial D_y}{\partial x} = \frac{D_{y\ (i+1,j+\frac{1}{2},k)}^{n+\frac{1}{2}} - D_{y\ (i,j+\frac{1}{2},k)}^{n+\frac{1}{2}}}{\delta x} \qquad \qquad \frac{\partial H_y}{\partial x} = \frac{H_{y\ (i+\frac{1}{2},j,k+\frac{1}{2})}^n - H_{y\ (i-\frac{1}{2},j,k+\frac{1}{2})}^n}{\delta x} \tag{5.23}$$

$$\frac{\partial D_z}{\partial x} = \frac{D_{z(i+1,j,k+\frac{1}{2})}^{n+\frac{1}{2}} - D_{z(i,j,k+\frac{1}{2})}^{n+\frac{1}{2}}}{\delta x} \qquad \qquad \frac{\partial H_z}{\partial x} = \frac{H_{z(i+\frac{1}{2},j+\frac{1}{2},k)}^n - H_{z(i-\frac{1}{2},j+\frac{1}{2},k)}^n}{\delta x}$$
(5.27)

$$\frac{\partial D_z}{\partial y} = \frac{D_{z\ (i,j+1,k+\frac{1}{2})}^{n+\frac{1}{2}} - D_{z\ (i,j,k+\frac{1}{2})}^{n+\frac{1}{2}}}{\delta y} \qquad \qquad \frac{\partial H_z}{\partial y} = \frac{H_{z\ (i+\frac{1}{2},j+\frac{1}{2},k)}^n - H_{z\ (i+\frac{1}{2},j-\frac{1}{2},k)}^n}{\delta y} \tag{5.29}$$

These equations can be used to develop a finite difference equation for $D_x^{n+\frac{1}{2}}_{x\ (i+\frac{1}{2},j,k)}$ from Equation 5.6 as given in Equation 5.30. The development of $D_{y\ (i,j+\frac{1}{2},k)}^{n+\frac{1}{2}}$ and $D_{z\ (i,j,k+\frac{1}{2})}^{n+\frac{1}{2}}$ proceeds in the same way. Similarly, a closed form for $H_{x\ (i,j+\frac{1}{2},k+\frac{1}{2})}^{n+\frac{1}{2}}$ based on Equation 5.9 with the aid of Equations 5.12–5.29 can be developed and is given in Equation 5.31. Again, the development of $H_{y\ (i+\frac{1}{2},j,k+\frac{1}{2})}^{n+\frac{1}{2}}$ and $H_{z\ (i+\frac{1}{2},j+\frac{1}{2},k)}^{n+\frac{1}{2}}$ proceeds in the same way.

$$D_{x\ (i+\frac{1}{2},j,k)}^{n+\frac{1}{2}} = D_{x\ (i+\frac{1}{2},j,k)}^{n-\frac{1}{2}} + \\ \delta t \frac{1}{\sqrt{\mu_0\epsilon_0}} \left(\frac{H_{z\ (i+\frac{1}{2},j+\frac{1}{2},k)}^n - H_{z\ (i+\frac{1}{2},j-\frac{1}{2},k)}^n}{\delta y} - \frac{H_{y\ (i+\frac{1}{2},j,k+\frac{1}{2})}^n - H_{y\ (i+\frac{1}{2},j,k-\frac{1}{2})}^n}{\delta z} \right)$$
(5.30)

$$H_{x(i,j+\frac{1}{2},k+\frac{1}{2})}^{n+1} = H_{x(i,j+\frac{1}{2},k+\frac{1}{2})}^{n} + \delta t \frac{1}{\sqrt{\mu_0 \epsilon_0}} \left(\frac{E_{y(i,j+\frac{1}{2},k+1)}^{n+\frac{1}{2}} - E_{y(i,j+\frac{1}{2},k)}^{n+\frac{1}{2}}}{\delta z} - \frac{E_{z(i,j+1,k+\frac{1}{2})}^{n+\frac{1}{2}} - E_{z(i,j,k+\frac{1}{2})}^{n+\frac{1}{2}}}{\delta y} \right)$$
(5.31)

The electric field $\vec{\mathbf{E}}$ (for use in Equation 5.31) can be obtained from $\vec{\mathbf{D}}$ (computed in Equation 5.30) by using the time domain $\vec{\mathbf{D}}-\vec{\mathbf{E}}$ relation derivable from Equation 5.3. Note that Equations 5.30–5.31 represent the general formulation for a numerical FDTD method in three dimensions for an infinite space. In order to reduce the computational complexity, the amount of required memory, and the simulation time, these preliminary simulations of thermal elevation are conducted in two dimensions. It is possible to approximate the fields generated by a three dimensional coil (as in the head/eye simulations for the retinal prosthesis) *via* a plane passing through its center and coplanar with the coil axis. Since the discretized models developed for this research are two dimensional, Equations 5.30–5.31 can be simplified to two dimensions by assuming no variation in the vector components of $\vec{\mathbf{E}}$ and $\vec{\mathbf{H}}$ along the *z*-axis (*k* index). That is, $\frac{\partial E_x}{\partial z} = 0$, $\frac{\partial E_y}{\partial z} = 0$, $\frac{\partial H_x}{\partial z} = 0$, and $\frac{\partial H_y}{\partial z} = 0$.

When assuming no variation in the z-direction, the six coupled vector components in Equations 5.6–5.11 can be separated into two sets of three coupled equations involving H_x , H_y , and E_z , called the *Transverse Magnetic Mode*, and E_x , E_y , and H_z , called the *Transverse Electric Mode*. Accordingly, the *Yee Cell* reduces to two dimensions for the two transverse modes as shown in Figure 5.2. For the two dimensional simulations of the head and eye conducted and summarized here, the transverse magnetic mode was used, as given in Equations 5.32–5.34 in the $\mathbf{\vec{D}}$ and $\mathbf{\vec{H}}$ formulation.

$$H_{x(i,j+\frac{1}{2})}^{n+1} = H_{x(i,j+\frac{1}{2})}^{n} - \delta t \frac{1}{\sqrt{\mu_0 \epsilon_0}} \left(\frac{E_{z(i,j+1)}^{n+\frac{1}{2}} - E_{z(i,j)}^{n+\frac{1}{2}}}{\delta y} \right)$$
(5.32)
$$H_{y(i+\frac{1}{2},j)}^{n+1} = H_{y(i+\frac{1}{2},j)}^{n} + \delta t \frac{1}{\sqrt{\mu_0 \epsilon_0}} \left(\frac{E_{z(i+1,j)}^{n+\frac{1}{2}} - E_{z(i,j)}^{n+\frac{1}{2}}}{\delta x} \right)$$
(5.33)

$$D_{z(i,j)}^{n+\frac{1}{2}} = D_{z(i,j)}^{n-\frac{1}{2}} + \delta t \frac{1}{\sqrt{\mu_0 \epsilon_0}} \left(\frac{H_y^n_{(i+\frac{1}{2},j)} - H_y^n_{(i-\frac{1}{2},j)}}{\delta x} - \frac{H_x^n_{(i,j+\frac{1}{2})} - H_x^n_{(i,j-\frac{1}{2})}}{\delta y} \right)$$
(5.34)



Figure 5.2: 2D dimensional equivalent of the Yee Cube for \vec{E} and \vec{H} vector assignments

5.2.1.2 Boundary conditions in the model space

Since the model space for simulating full wave propagation and penetration defines a finite area or volume, the waves emitted from the source may and typically do encounter the boundary of the space. If not properly taken into account, the wave will reflect from the boundary and will propagate back into the model space, where it will subsequently re-encounter the model, or body, under consideration. The technique which has been devised to deal with this problem is call the *Perfectly Matched Layer*, or PML [136], [137]. Conceptually, this represents a layer of fictitious material surrounding the model space, which is impedance matched to the vacuum $\left(\eta_0 = \sqrt{\frac{\mu_0}{\epsilon_0}}\right)$ but which also presents a gradual and progressively increasing conductivity to waves reaching the boundary. This conductivity increases exponentially in proportion to the penetration depth into the PML, such that wave energy is absorbed with no reflected wave allowed to re-enter the model space. The mathematical development of the PML is integrally performed in the discretization and is not simply added to the discretized formulations of Equations 5.30–5.31. The discretization to include the PML is performed in $\vec{\mathbf{D}}$ and $\vec{\mathbf{H}}$ rather than in $\vec{\mathbf{E}}$ and $\vec{\mathbf{H}}$, as the *D*-*H* formulation has the advantage that the Perfectly Matched Layer (PML) absorbing boundary conditions are independent from the background dielectric materials in the FDTD mesh (both in 2D and 3D formulations). The derivation proceeds from the vector component relations of Equations 5.6–5.11 with the time derivatives of $\frac{\partial D_x}{\partial t}$, $\frac{\partial D_y}{\partial t}$, $\frac{\partial D_z}{\partial t}$, $\frac{\partial H_x}{\partial t}$, $\frac{\partial H_y}{\partial t}$, and $\frac{\partial H_z}{\partial t}$ expressed in the frequency domain as $j\omega D_x$, $j\omega D_y$, $j\omega D_z$, $j\omega H_x$, $j\omega H_y$, and $j\omega H_z$, respectively. Thus, the derivation of a 3D FDTD implementation with PML absorbing boundary conditions closely follows that in [136] and uses modified Maxwell's equations to account for the fictitious material:

$$j\omega\left(1+\frac{\sigma_x(x)}{j\omega\epsilon_0}\right)^{-1}\left(1+\frac{\sigma_y(y)}{j\omega\epsilon_0}\right)\left(1+\frac{\sigma_z(z)}{j\omega\epsilon_0}\right)D_x = \frac{1}{\sqrt{\mu_0\epsilon_0}}\left(\frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z}\right) \quad (5.35)$$

$$j\omega\left(1+\frac{\sigma_x(x)}{j\omega\epsilon_0}\right)\left(1+\frac{\sigma_y(y)}{j\omega\epsilon_0}\right)^{-1}\left(1+\frac{\sigma_z(z)}{j\omega\epsilon_0}\right)D_y = \frac{1}{\sqrt{\mu_0\epsilon_0}}\left(\frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x}\right) \quad (5.36)$$

$$j\omega\left(1+\frac{\sigma_x(x)}{j\omega\epsilon_0}\right)\left(1+\frac{\sigma_y(y)}{j\omega\epsilon_0}\right)\left(1+\frac{\sigma_z(z)}{j\omega\epsilon_0}\right)^{-1}D_z = \frac{1}{\sqrt{\mu_0\epsilon_0}}\left(\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y}\right) \quad (5.37)$$

$$j\omega\left(1+\frac{\sigma_x(x)}{j\omega\epsilon_0}\right)^{-1}\left(1+\frac{\sigma_y(y)}{j\omega\epsilon_0}\right)\left(1+\frac{\sigma_z(z)}{j\omega\epsilon_0}\right)H_x = \frac{1}{\sqrt{\mu_0\epsilon_0}}\left(\frac{\partial E_y}{\partial z} - \frac{\partial E_z}{\partial y}\right) \quad (5.38)$$

$$j\omega\left(1+\frac{\sigma_x(x)}{j\omega\epsilon_0}\right)\left(1+\frac{\sigma_y(y)}{j\omega\epsilon_0}\right)^{-1}\left(1+\frac{\sigma_z(z)}{j\omega\epsilon_0}\right)H_y = \frac{1}{\sqrt{\mu_0\epsilon_0}}\left(\frac{\partial E_z}{\partial x} - \frac{\partial E_x}{\partial z}\right) \quad (5.39)$$

$$j\omega\left(1+\frac{\sigma_x(x)}{j\omega\epsilon_0}\right)\left(1+\frac{\sigma_y(y)}{j\omega\epsilon_0}\right)\left(1+\frac{\sigma_z(z)}{j\omega\epsilon_0}\right)^{-1}H_z = \frac{1}{\sqrt{\mu_0\epsilon_0}}\left(\frac{\partial E_x}{\partial y} - \frac{\partial E_y}{\partial x}\right) \quad (5.40)$$

From these frequency domain equations it is possible to derive the time domain expressions for $\vec{\mathbf{D}}$ and $\vec{\mathbf{H}}$ which include the PML materials. The exponentially increasing conductivity which absorbs electromagnetic waves incident on the PML is represented by the spatial functions, $\sigma_x(x)$, $\sigma_y(y)$, and $\sigma_z(z)$ [138], [139]. Note that these do not account for the conductivities of the tissues in the head and eye models. The electromagnetic FDTD implementation used here incorporates the PML absorbing boundaries such that the head and eye model can be truncated with appropriate treatment for reflections as described in [136] in order to limit the computational space. As the mathematical development of the PML is lengthy and closely parallels that in [136] and [140], the details of further derivation are deferred to [136], [137], and [141] and in the sake of brevity will not be repeated here.

5.2.2 Finite difference time domain simulation of temperature distribution

The flow of heat in a solid material is expressed by the classical heat equation [142]:

$$\frac{\partial T}{\partial t} = a^2 \nabla^2 T = a^2 \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right)$$
(5.41)

where T is temperature as a function of time, t, and spatial coordinates (x,y,z) and the thermal diffusivity, a^2 , is defined in terms of thermal conductivity, K, specific heat, C, and mass density, ρ , as $a^2 = \frac{K}{C\rho}$.

When considering biological tissue, the heat equation is expanded as in Equation 5.42 to include basal metabolism, A_0 , which has the effect of raising the temperature, and the cooling effect of blood perfusion, B, in the tissue. T_b is the blood temperature which is assumed constant at 37°C. This is referred to as the "bio-heat equation" [122].

$$C\rho \frac{\partial T}{\partial t} = K\nabla^2 T + A_0 - B(T - T_b) \quad \left[\frac{W}{m^3}\right]$$
(5.42)

The blood perfusion constant is further defined as in Equation 5.43, where ρ_b is the mass density of blood, C_b is the specific heat of blood, ρ_t is the mass density of the tissue perfused with blood, and m_b is the mass flow rate of blood in the tissue, expressed as a volume per unit time for a given mass of tissue.

$$B = \rho_t \rho_b C_b m_b \quad \left[\frac{W}{m^3 \circ C}\right] \tag{5.43}$$

When considering tissue which is irradiated electromagnetically, the bio-heat equation is further expanded to include the temperature raising effect of the specific absorption rate, SAR, in units of $\begin{bmatrix} W\\ kg \end{bmatrix}$. The specific absorption rate is a measure of absorbed power per unit mass of tissue due to exposure to electromagnetic fields, and is expressed as $SAR = \frac{\sigma ||\vec{\mathbf{E}}||^2}{2\rho}$, for conductivity, σ , electric field, $\vec{\mathbf{E}}$, and mass density, ρ . Furthermore, the power dissipation in the stimulator IC, $P_{chip(3D)}$ in units of [W], which also raises tissue temperature, is included as given in Equation 5.44 where it is expressed as a power dissipation density, $P_{\substack{chip(3D)\\(\text{continuous})}}^{(density)}$ in units of $\left[\frac{W}{m^3}\right]$.

$$C\rho \frac{\partial T}{\partial t} = K\nabla^2 T + A_0 - B(T - T_b) + \rho SAR_{(x,y,z)} + P_{\substack{chip(3D)\\(\underline{continuous})}}^{(density)} \left[\frac{W}{m^3}\right] , \quad (5.44)$$

where the thermal properties, computed temperature, SAR and stimulator IC power dissipation are all implicitly functions of the continuous 3D space (*ie-* $\rho = \rho(x, y, z)$, C = C(x, y, z), K = K(x, y, z), etc.), but are shown with simplified notation for clarity.

At the boundary of the tissue where the surrounding environment is encountered, the conduction of heat through the tissue arriving at the boundary normal to the surface must match the convective transfer of heat into the environment [122]. The exchange of heat with the surrounding environment is proportional to the difference between the surface temperature and the environmental temperature as given in Equation 5.45 [122], [127]

$$K\frac{\partial T}{\partial n}(x,y,z) = -H_a(T_{(x,y,z)} - T_a) \quad \left[\frac{W}{m^2}\right] , \qquad (5.45)$$

where $T_{(x,y,z)}$ is evaluated on the surface, H_a is the constant environmental ambient convection coefficient given in units of $\left[\frac{J}{m^2 \ s \ \circ C}\right]$, and T_a is the constant environmental ambient temperature.

As was done with the Maxwell's equations in Section 5.2.1, the bio-heat equation is discretized over time and space as depicted in Figure 5.3 in order to arrive at a formulation suitable for implementation on a computer.

Finite difference approximations for first derivative over time, $\frac{\partial T}{\partial t}$, and the second derivatives over space, $\frac{\partial^2 T}{\partial x^2}$, $\frac{\partial^2 T}{\partial y^2}$, and $\frac{\partial^2 T}{\partial z^2}$ (from $\nabla^2 T$), can be developed and are

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Figure 5.3: Spatial discretization in the formulation of the 3D thermal numerical method

given in Equations 5.46–5.52.

$$\frac{\partial T}{\partial t} = \frac{T_{(i,j,k)}^{n+1} - T_{(i,j,k)}^n}{\delta t}$$
(5.46)

$$\frac{\partial T}{\partial x} = \frac{T_{(i+1,j,k)}^n - T_{(i,j,k)}^n}{\delta x} \tag{5.47}$$

$$\frac{\partial T}{\partial y} = \frac{T_{(i,j+1,k)}^n - T_{(i,j,k)}^n}{\delta y} \tag{5.48}$$

$$\frac{\partial T}{\partial z} = \frac{T_{(i,j,k+1)}^n - T_{(i,j,k)}^n}{\delta z} \tag{5.49}$$

 ∂y^2

$$\frac{\partial^2 T}{\partial x^2} = \frac{\partial}{\partial x} \left(\frac{\partial T}{\partial x} \right) = \frac{\frac{T_{(i+1,j,k)}^n - T_{(i,j,k)}^n}{\delta x} - \frac{T_{(i,j,k)}^n - T_{(i-1,j,k)}^n}{\delta x}}{\delta x}$$
(5.50)
$$= \frac{T_{(i+1,j,k)}^n + T_{(i-1,j,k)}^n - 2T_{(i,j,k)}^n}{\delta x^2}$$

$$\frac{\partial^2 T}{\partial x^2} = \frac{T_{(i,j+1,k)}^n + T_{(i,j-1,k)}^n - 2T_{(i,j,k)}^n}{\delta x^2}$$
(5.51)

 δy^2

$$\frac{\partial^2 T}{\partial z^2} = \frac{T_{(i,j,k+1)}^n + T_{(i,j,k-1)}^n - 2T_{(i,j,k)}^n}{\delta z^2}$$
(5.52)

By using these approximations, the continuous time equations for bio-heat conduction of Equation 5.44 and the convection boundary condition of Equation 5.45 can be discretized and combined as reported in [122] and given in Equation 5.53. In keeping with Equation 5.44, specific absorption rate from inductive coupling, $SAR_{(x,y,z)}$, and the power dissipation density for the stimulator IC, $P_{chip(3D)}^{(density)}$, have been included. (continuous)

$$\begin{split} T_{(i,j,k)}^{n+1} = & \frac{K\delta t}{\rho C\delta x^2} \left(T_{(i-1,j,k)}^n + T_{(i+1,j,k)}^n + T_{(i,j-1,k)}^n + T_{(i,j+1,k)}^n + T_{(i,j,k-1)}^n + T_{(i,j,k+1)}^n \right) + \\ & T_{(i,j,k)}^n \left[1 - \left(N_{INT} \frac{K}{\rho C\delta x^2} + N_{EXT} \frac{H_a}{\rho C\delta x} + \frac{B}{\rho C} \right) \delta t \right] + N_{EXT} \frac{H_a \delta t T_a}{\rho C\delta x} + \\ & \frac{\delta t}{\rho C} \left[\rho SAR_{(i,j,k)} + P_{chip(3D)}^{(density)}(i,j,k) + A_{0_{(i,j,k)}} + B_{(i,j,k)} T_b} \right], \text{ where} \\ & \delta x = \delta y = \delta z \;, \end{split}$$
(5.53)

where N_{INT} is the number of interior points adjacent to cell (i, j, k) and N_{EXT} is the number of exterior points adjacent to cell (i, j, k) (ie- those outside of the model and belonging to the surrounding environment). The thermal properties, computed temperature, SAR and stimulator IC power dissipation are now implicitly functions of the 3D discretized model space (*ie-* $\rho = \rho(i, j, k)$, C = C(i, j, k), K = K(i, j, k), etc.), but are again shown with simplified notation for clarity. In order to ensure stability in the numerical thermal method, the maximum time step is related to the spatial discretization of the model, the thermal properties of the tissues, blood perfusion in the tissues, and the convective heat transfer properties with the environment. The maximum time step to ensure stability of the algorithm is considered as the minimum value of the expression of Equation 5.54 when considering all tissues and materials present in the discretized model. It is worth noting that the silicon and metallic properties of the implant have thermal conductivities two to three orders of magnitude higher that that of body tissues. This imposes a much smaller time step for stable execution of the method.

$$\delta t \le \min_{n \in N} \left(\frac{1}{\frac{N_{INT}K_n}{\rho_n C_n \delta x^2} + \frac{N_{EXT}H_a}{\rho_n C_n \delta x} + \frac{B_n}{\rho_n C_n}} \right), \text{ where N is the set tissues}$$
(5.54)

Note that Equation 5.53 represents the general formulation for a time-domain thermal method in three dimensions. Again, the discretized models developed for this research are two dimensional. Therefore, Equation 5.53 can be simplified to two dimensions by assuming no variation of temperature along the z-axis (k index). Thus, the spatial discretization of Figure 5.3 simplifies to the form illustrated in Figure 5.4. Each cell of the model will have at most 4 interior neighbors (-i, +i, -j, +j) instead of six in the case of the three dimensional method (-i, +i, -j, +j, -k, +k). Accordingly, Equation 5.53 reduces to the form given in Equation 5.55.



Figure 5.4: Spatial discretization in the formulation of the 2D thermal numerical method

$$T_{(i,j)}^{n+1} = \frac{K\delta t}{\rho C \delta x^2} \left(T_{(i-1,j)}^n + T_{(i+1,j)}^n + T_{(i,j-1)}^n + T_{(i,j+1)}^n \right) + T_{(i,j)}^n \left[1 - \left(N_{INT} \frac{K}{\rho C \delta x^2} + N_{EXT} \frac{H_a}{\rho C \delta x} + \frac{B}{\rho C} \right) \delta t \right] + N_{EXT} \frac{H_a \delta t T_a}{\rho C \delta x} + \frac{\delta t}{\rho C} \left[\rho SAR_{(i,j)} + P_{chip(2D)}^{(density)}(i,j) + A_{0_{(i,j)}} + B_{(i,j)} T_b} \right], \text{ where} \\ \frac{\delta t}{\delta x} = \delta y$$

$$(5.55)$$

Equations 5.54–5.55 are used to calculate the temperature rise in the eye when exposed to electromagnetic radiation from inductive coupling and under the operation of the implanted stimulator microchip. The parameters used in these equations together with their units are summarized in table 5.1.

5.2.3 Justification of the simplified thermal conduction term

The bio-heat formulation given in Equation 5.44, which was expanded with terms for SAR and power density suitable for accomodating thermal simulations of the

Symbol	Physical Property	Units
T	Temperature	$^{\circ}C$
t	continuous time	s
n	surface normal	—
ρ	mass density	$\left[\frac{kg}{m^3}\right]$
C	specific heat	$\left[\frac{J}{kg^{\circ}C}\right]$
K	thermal conductivity	$\left[\frac{J}{m \circ C}\right]$
H_a	convective transfer constant	$\left[\frac{m^2 s^{\circ} C}{m^2 s^{\circ} C}\right]$
	(for environmental ambient temperature)	111 3 0 1
A_0	basal metabolic rate	$\left[\frac{J}{m^3s}\right]$
В	blood perfusion constant	$\left[\frac{J}{m^3 s^\circ C}\right]$
m_b	blood mass flow rate	$\left[\frac{m^3}{s \ kg}\right]$
T_b	blood temperature (constant)	$\circ C$
T_a	environment ambient temperature (constant)	$^{\circ}C$
δx	spatial step (resolution) in the x, i direction	m
δy	spatial step (resolution) in the y, j direction	m
δz	spatial step (resolution) in the z, k direction	m
δt	discretized time step	s
SAR	specific absorption rate	$\left[\frac{W}{kg}\right]$
$P_{chip(3D)}^{(density)}$	power dissipation density for the stimulator IC	$\left[\frac{W}{m^3}\right]$

Table 5.1: Parameters in the bio-heat equation

stimulator IC, manifests a simplification for spatial thermal conduction. For models in which the thermal conductivity, K, is constant, the conduction term is $K\nabla^2 T$. However, for models in which thermal conductivity is spatially variant then the more correct term becomes $\nabla (K\nabla T)$ which yields the more generalized form of the bioheat equation given in Equation 5.56.

$$C\rho \frac{\partial T}{\partial t} = \nabla \left(K\nabla T\right) + A_0 - B(T - T_b) + \rho SAR_{(x,y,z)} + \frac{P_{chip(3D)}^{(density)}}{(continuous)} \left[\frac{W}{m^3}\right]$$
(5.56)

From recent prior work [122], [127] involving electromagnetic dosimetry from cellular phones applied to human head/eye models, the use the simplified conduction term of $K\nabla^2 T$ appeared justifiable because the thermal conductivities of the head/eye tissues vary only slighly around values of 0.5 $\left[\frac{J}{m \ s \ \circ C}\right]$. This allows the thermal conductivity, K, to be approximated as constant and subsequently factored out of $\nabla (K\nabla T)$ to yield $K\nabla^2 T$. For the retinal prosthesis, the presence of the silicon retinal stimulator IC with much higher thermal conductivity of $K_{SI} = 150$ invalidates this simplification since K within the eye region now becomes spatially variant.

In order to justify the use of $K\nabla^2 T$ in these studies of thermal elevation associated with the retinal prosthesis, the results of the two numerical methods in two dimensions based on $K\nabla^2 T$ and $\nabla (K\nabla T)$, respectively, are compared to the numerical method in three dimensions based on $\nabla (K\nabla T)$. In order to ease the computational burden of this comparison, a much smaller model is derived for these simulations, since the three dimensional simulation is particularly processor and memory intensive. The simplified model for this study consists of 80x80 cells (80x80x80 in three dimensions) containing a sphere of radius 38 cells of uniform material composition having the thermal properties of muscle tissue provided in Table 5.6. The same chip model of 22x21x2 cells developed in Section 5.5.2 (with $K_{chip} = 10$ for reducing the computational time) was placed in the center and excited with the worst-case power of 46.4672 mW.

In further support of the comparison, the generalized bio-heat formulation of Equation 5.56 is now discretized in space and time in the same manner as done for Equation 5.44 in Section 5.2.2. The generalized thermal conduction term is now expanded as given in Equation 5.57,

$$\nabla (K\nabla T) = \nabla \left(K \frac{\partial T}{\partial x} \vec{\mathbf{i}} + K \frac{\partial T}{\partial y} \vec{\mathbf{j}} + K \frac{\partial T}{\partial z} \vec{\mathbf{k}} \right)$$

$$= \frac{\partial}{\partial x} \left(K \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left(K \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left(K \frac{\partial T}{\partial z} \right)$$

$$= K \frac{\partial^2 T}{\partial x^2} + K \frac{\partial^2 T}{\partial y^2} + K \frac{\partial^2 T}{\partial z^2} + \frac{\partial K}{\partial x} \frac{\partial T}{\partial x} + \frac{\partial K}{\partial y} \frac{\partial T}{\partial y} + \frac{\partial K}{\partial z} \frac{\partial T}{\partial z}$$
(5.57)

whereas formerly:

$$K\nabla^2 T = K \frac{\partial^2 T}{\partial x^2} + K \frac{\partial^2 T}{\partial y^2} + K \frac{\partial^2 T}{\partial z^2}$$
(5.58)

The finite difference form of the spatial derivatives of temperature are the same as those given in Equations 5.47–5.52, where as the spatial derivatives of thermal conductivity are given as:

$$\frac{\partial K}{\partial x} = \frac{K_{(i+1,j,k)} - K_{(i,j,k)}}{\delta x}$$
(5.59)

$$\frac{\partial K}{\partial y} = \frac{K_{(i,j+1,k)} - K_{(i,j,k)}}{\delta y}$$
(5.60)

$$\frac{\partial K}{\partial z} = \frac{K_{(i,j,k+1)} - K_{(i,j,k)}}{\delta z} \tag{5.61}$$

Accordingly, the generalized thermal conduction term expands to a finite difference

form as given in Equation 5.62.

$$\nabla (K\nabla T) = K_{(i,j,k)} \left(\frac{T_{(i+1,j,k)}^{n} + T_{(i-1,j,k)}^{n} - 2T_{(i,j,k)}^{n}}{\delta x^{2}} \right) + K_{(i,j,k)} \left(\frac{T_{(i,j+1,k)}^{n} + T_{(i,j-1,k)}^{n} - 2T_{(i,j,k)}^{n}}{\delta y^{2}} \right) + K_{(i,j,k)} \left(\frac{T_{(i,j,k+1)}^{n} + T_{(i,j,k-1)}^{n} - 2T_{(i,j,k)}^{n}}{\delta z^{2}} \right) + \left(\frac{K_{(i+1,j,k)} - K_{(i,j,k)}}{\delta x} \right) \left(\frac{T_{(i+1,j,k)}^{n} - T_{(i,j,k)}^{n}}{\delta x} \right) + \left(\frac{K_{(i,j+1,k)} - K_{(i,j,k)}}{\delta y} \right) \left(\frac{T_{(i,j+1,k)}^{n} - T_{(i,j,k)}^{n}}{\delta y} \right) + \left(\frac{K_{(i,j,k+1)} - K_{(i,j,k)}}{\delta z} \right) \left(\frac{T_{(i,j,k+1)}^{n} - T_{(i,j,k)}^{n}}{\delta z} \right) \right)$$
(5.62)

For equal cell dimensions in the x, y, and z directions, $\delta x = \delta y = \delta z$, this simplifies to:

$$\nabla \left(K \nabla T \right) = \left(\frac{K_{(i+1,j,k)} T_{(i+1,j,k)}^n + K_{(i,j+1,k)} T_{(i,j+1,k)}^n + K_{(i,j,k+1)} T_{(i,j,k+1)}^n}{\delta x^2} \right) + K_{(i,j,k)} \left(\frac{T_{(i-1,j,k)}^n + T_{(i,j-1,k)}^n + T_{(i,j,k-1)}^n}{\delta x^2} \right) - T_{(i,j,k)}^n \left(\frac{K_{(i+1,j,k)} + K_{(i,j+1,k)} + K_{(i,j,k+1)} + 3K_{(i,j,k)}}{\delta x^2} \right)$$
(5.63)

Expanding the finite difference formulation of Equation 5.53 with this derivation to account for the generalized conduction term in lieu of Equation 5.56 yields the finite difference numerical thermal method of Equation 5.64 in three dimensions which includes spatial gradients in the thermal conductivity, K.

$$\begin{split} T_{(i,j,k)}^{n+1} = & \frac{\delta t}{\rho C \delta x^2} \bigg(K_{(i,j,k)} T_{(i-1,j,k)}^n + K_{(i+1,j,k)} T_{(i+1,j,k)}^n + K_{(i,j,k)} T_{(i,j-1,k)}^n + \\ & K_{(i,j+1,k)} T_{(i,j+1,k)}^n + K_{(i,j,k)} T_{(i,j,k-1)}^n + K_{(i,j,k+1)} T_{(i,j,k+1)}^n \bigg) + \\ & T_{(i,j,k)}^n \bigg[1 - \bigg(N_{INT} \bigg(\frac{K_{(i+1,j,k)} + K_{(i,j+1,k)} + K_{(i,j,k+1)} + 3K_{(i,j,k)}}{\rho C \delta x^2} \bigg) + \\ & N_{EXT} \frac{H_a}{\rho C \delta x} + \frac{B}{\rho C} \bigg) \delta t \bigg] + N_{EXT} \frac{H_a \delta t T_a}{\rho C \delta x} + \\ & \frac{\delta t}{\rho C} \bigg[\rho S A R_{(i,j,k)} + P_{chip(3D)}^{(density)}(i,j,k) + A_{0_{(i,j,k)}} + B_{(i,j,k)} T_b} \bigg], \text{ where} \\ & \delta x = \delta y = \delta z \\ & (5.64) \end{split}$$

The two dimensional form follows from this by assuming no variation in the z, or k, direction and is given by:

$$\begin{split} T_{(i,j)}^{n+1} = & \frac{\delta t}{\rho C \delta x^2} \left(K_{(i,j)} T_{(i-1,j)}^n + K_{(i+1,j)} T_{(i+1,j)}^n + K_{(i,j)} T_{(i,j-1)}^n + K_{(i,j+1)} T_{(i,j+1)}^n \right) + \\ & T_{(i,j)}^n \left[1 - \left(N_{INT} \left(\frac{K_{(i+1,j)} + K_{(i,j+1)} + 2K_{(i,j)}}{\rho C \delta x^2} \right) + \right. \\ & \left. N_{EXT} \frac{H_a}{\rho C \delta x} + \frac{B}{\rho C} \right) \delta t \right] + N_{EXT} \frac{H_a \delta t T_a}{\rho C \delta x} + \\ & \frac{\delta t}{\rho C} \left[\rho SAR_{(i,j)} + \frac{P_{chip(2D)}^{(density)}}{(discrete)}(i,j) + A_{0_{(i,j)}} + B_{(i,j)} T_b \right], \text{ where} \\ & \delta x = \delta y \end{split}$$
(5.65)

Results show that the numerical method based on the $\nabla (K\nabla T)$ conduction term in two dimensional simulations produces an unphysically high temperature increase near the interface between the microchip and the eye's vitreous humor. This is not observed in three dimensional simulations based on the same conduction term. This is essentially due to the fact that in two dimensions, heat cannot dissipate in the z, or k, direction. The two dimensional simulation based on the $K\nabla^2 T$ conduction term yields results which are in much better agreement with those from the three dimensional simulation involving $\nabla (K\nabla T)$. Results are shown in Figure 5.5 for the two dimensional $K\nabla^2 T$ simulation and in Figure 5.6 for the three dimensional $\nabla (K\nabla T)$ simulation. The 3D case shows, as expected, slightly faster temperature decay with increasing distance from the center of the stimulator IC. As further discussed in Section 5.7, the two dimensional assumptions involving the use of the $K\nabla^2 T$ conduction term have been validated by means of a number of *in-vivo* experiments performed at the USC medical school, which show high correlation between the simulated numerical data and the experimental measurements.



(a) Temperature increase at the center of the chip



Heating in the 80x80 (2D) model from 46.5mW in the chip

(b) Distribution of thermal elevation across the center of the model

Figure 5.5: $K\nabla^2 T$ in 2D simulation



(a) Temperature increase at the center of the chip



Heating in the 80x80x80 (3D) model from 46.5mW in the chip

(b) Distribution of thermal elevation across the center of the model

Figure 5.6: $\nabla(K\nabla T)$ in 3D simulation

5.3 Validation of the FDTD and thermal methods

Numerical, iterative methods such as these are prone to accumulated errors, instabilities, or incorrect mathematical derivation or implementation. Therefore, a validation is necessary in order to confirm that the method accurately represents the physical process. This is typically performed by comparing the method's predictions with those obtained analytically for a simple problem.

In [143], the authors have developed an analytical solution for the specific absorption rate and the thermal response associated with a plane wave impacting a solid cylinder with the dielectric and thermal properties of muscle, as illustrated in Figure 5.7.



Figure 5.7: Plane wave impacting a circular cylinder

The analytical solution for SAR and temperature can be evaluated for any frequency and incident plane wave power and with any dielectric or thermal properties. In their published work, the analytical solution was evaluated at 2.45GHz. In this study, where the implanted micro-stimulator will be inductively powered, the frequency of excitation will be three orders of magnitude lower. Accordingly, a value of 2MHz has been chosen. Therefore, the validation of the FDTD and thermal implementations will be performed at the frequency of 2.45GHz reported in [143] in order to compare with the published results as well as at 2MHz.

5.3.1 Electromagnetic (SAR) validation

5.3.1.1 Analytical simulation

In [143], the specific absorption rate resulting from the plane wave of incident power, P_0 , impacting the cylinder model as in Figure 5.7 is formulated as

$$SAR(r,\theta) = \begin{cases} 0 & \text{for } t < 0, \\ \frac{\sigma}{2\rho} \vec{\mathbf{E}}(r,\theta) \vec{\mathbf{E}}^*(r,\theta) & \text{for } t \ge 0. \end{cases}$$
(5.66)

The Electric Field, $\vec{\mathbf{E}}$, is directed along the axis of the cylinder and at an arbitrary polar location of (r,θ) within the cylinder and is given by Equation 5.67 [143].

$$\vec{\mathbf{E}}(r,\theta) = \vec{\mathbf{z}}E_z(r,\theta) = \vec{\mathbf{z}}E_0\sum_{n=0}^{\infty}Q_n J_n(kr)\cos(n\theta)$$
(5.67)

where E_0 and Q_n defined as in Equations 5.68–5.69 [143].

$$E_0 = \sqrt{2\eta_0 P_0}, \text{ for } \eta_0 = \sqrt{\frac{\mu_0}{\epsilon_0}}$$
 (5.68)

$$Q_n = \frac{j^{-(n+1)}2(2-\delta_{0n})}{\pi r_0 \left[k_0 J_n(kr_0) H_n^{(2)'}(k_0r_0) - k J_n'(kr_0) H_n^{(2)}(k_0r_0) \right]}$$
(5.69)

with

$$k^2 = k_0^2 \epsilon_{cr}, \quad \text{and} \tag{5.70}$$

$$k_0 = \omega \sqrt{\epsilon_0 \mu_0}, \quad \text{for } \omega = 2\pi f, \text{ and}$$
 (5.71)

$$\epsilon_{cr} = \frac{\epsilon}{\epsilon_0} - \frac{j\sigma}{\omega\epsilon_0}, \quad \text{for } \omega = 2\pi f.$$
 (5.72)

5.3.1.2 Numerical simulation

The numerical approach to computing SAR on the irradiated cylinder from [143] proceeds with the mathematical discretization of Maxwell's equations from Section 5.2.1.1. The numerical simulation of the cylinder considers a spatially discretized model space consisting of the 2D cylindrical cross section surrounded with PML absorbing boundaries as described in Section 5.2.1.2. This is illustrated in Figure 5.8. The numerical method is formulated using the *Transverse Magnetic* mode, based on Equations 5.32– 5.34.

5.3.1.3 Comparison at 2.45GHz irradiation

The parameters used to compute the SAR resulting from exposure of the cylinder to the 2.45GHz plane wave are summarized in Table 5.2 [143]. The comparison of the analytically computed SAR to the numerically computed SAR is plotted in Figure 5.9a. The analytical solution is represented by the continuous curve plotted as a function of the wave penetration depth into the cylinder. In the numerical method a cylinder model with 100 cells across the radius corresponding to a "real" radius of $r_0 = 0.05$ m is used. The overlayed discrete points represent the predicted SAR from the numerical FDTD method taken at cells along the cylinder diameter perpendicular to the plane wave. As expected, both the analytical and numerical solutions diminish rapidly in the cylinder due to higher conductivity at 2.45GHz. A color-mapped two dimensional cross section of the SAR obtained from the numerical FDTD is provided in Figure 5.9b.



Figure 5.8: 2D model space of the irradiated cylinder with PML boundaries

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Symbol	Physical Property	Value	Units
r_0	cylinder radius	0.05	m
P_0	plane wave incident power density	1000	$\left[\frac{W}{m^2}\right]$
f	plane wave frequency	2.45	GHz
ϵ_r	relative permittivity	47	—
σ	conductivity	2.21	$\left[\frac{S}{m}\right]$
ρ	mass density	1070	$\left[\frac{kg}{m^3}\right]$
δx	Resolution of the cylinder model	0.5	mm
N_{PML}	Number of cells in the PML layer	16	—
I_{max}	Number of rows in the 2D FDTD space	220	—
	(excluding PML layer at top and bottom)		
J_{max}	Number of columns in the 2D model space	220	—
	(excluding PML layer at left and right)		

Table 5.2: Parameters for the SAR validation at 2.45GHz



(b) Numerical SAR distribution

Figure 5.9: Specific absorption rate in the test cylinder at 2.45GHz irradiation

5.3.1.4 Comparison at 2MHz irradiation

A similar comparison between the analytical and numerical SAR solutions is conducted for the case of a 2MHz plane wave irradiating the cylinder model. The parameters which are used to compute the SAR for the 2MHz plane wave are summarized in Table 5.3. The resulting SAR is plotted in Figure 5.10a. As in the 2.45GHz case, a cylinder model with 100 cells across the radius corresponding to a radius of $r_0 = 0.05$ m is used. Once again, the analytical solution is represented by the continuous curve plotted as a function of the wave penetration depth into the cylinder with the overlayed discrete points representing the predicted SAR from the numerical FDTD.

At 2MHz, the computed SAR shows a greater penetration depth into the cylinder, owing partially to lower conductivity at 2MHz, but also due to the longer wavelength (150m at 2MHz) with respect to the dimension of the scattering object represented by the cylinder. A color-mapped two dimensional cross section of the SAR obtained from the numerical FDTD is provided in Figure 5.10b.

Symbol	Physical Property	Value	Units
r_0	cylinder radius	0.05	m
P_0	plane wave incident power density	10	$\left[\frac{W}{m^2}\right]$
f	plane wave frequency	2	MHz
ϵ_r	relative permittivity	850	_
σ	conductivity	1	$\left[\frac{S}{m}\right]$
ρ	mass density	1070	$\left[\frac{kg}{m^3}\right]$
δx	Resolution of the cylinder model	0.5	mm
N_{PML}	Number of cells in the PML layer	40	_
I_{max}	Number of rows in the 2D FDTD space	220	_
	(excluding PML layer at top and bottom)		
J_{max}	Number of columns in the 2D model space	220	_
	(excluding PML layer at left and right)		

Table 5.3: Parameters for the SAR validation at 2MHz



(b) Numerical SAR distribution

Figure 5.10: Specific absorption rate in the test cylinder at 2MHz irradiation

5.3.2 Thermal validation

The analytical and numerical thermal responses of the muscle cylinder to the plane wave irradiation follow from the SAR computed analytically and numerically as described in Section 5.3.1 [122], [143]. Once again, analysis at the frequency of 2.45GHz reported in [122] is considered as well as at 2MHz for the retinal prosthesis.

5.3.2.1 Analytical simulation

In [143], the thermal response of the cylinder model of Figure 5.7 to the impacting plane wave of incident power, P_0 , is formulated in Equation 5.73 [143] for arbitrary polar location of (r, θ) within the cylinder and at time, t.

$$T(r,\theta,t) = v(r,\theta,t) + \nu_e \tag{5.73}$$

The temperature, $T(r, \theta, t)$, is further defined in terms of a thermal increase of $v(r, \theta, t)$ above the fixed environmental ambient temperature (*ie*-air) of ν_e . This thermal increase is further expanded as

$$v(r,\theta,t) = \begin{cases} u_0(r,\theta) & \text{for } t < 0, \\ u_0(r,\theta) + u_1(r,\theta) + w(r,\theta,t) & \text{for } t \ge 0. \end{cases}$$
(5.74)

where $u_0(r, \theta)$ represents the initial temperature distribution above the environmental temperature, ν_e , in the cylinder at a location of (r, θ) prior to plane wave irradiation, $u_1(r, \theta)$ represents the final value of the temperature increase, and $w(r, \theta, t)$ represents the time-variant increase in temperature about the initial distribution [143]. These three components are further defined in Equations 5.75–5.77 [143].

$$u_0(r,\theta) = \frac{a_0}{b^2} \left[1 - \frac{J_0(jbr)}{J_0(jbr_0) + j\frac{b}{h}J_0'(jbr_0)} \right]$$
(5.75)

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$$u_1(r,\theta) = \sum_{n=0}^{\infty} \sum_{m=1}^{\infty} (2 - \delta_{0n}) U_{1nm} f_{nm}(r,\theta)$$
(5.76)

$$w(r,\theta,t) = -\sum_{n=0}^{\infty} \sum_{m=1}^{\infty} (2-\delta_{0n}) U_{1nm} f_{nm}(r,\theta) e^{-\kappa(\lambda_{nm}^2+b^2)t}$$
(5.77)

Thus, the absolute initial temperature in the cylinder is represented by $\nu_e + u_0(r, \theta)$. Since $u_1(r, \theta)$ represents the final value of the **temperature increase** above the initial temperature of $\nu_e + u_0(r, \theta)$, the steady state temperature distribution is given by $\nu_e + u_0(r, \theta) + u_1(r, \theta)$. At the initial time of t = 0, $w(r, \theta, t) = -u_1(r, \theta)$, such that $T(r, \theta, t) = u_0(r, \theta) + \nu_e$ for t = 0. As $t \to \infty$, $w(r, \theta, t) \to 0$, such that $T(r, \theta, t) \to u_0(r, \theta) + u_1(r, \theta) + \nu_e$.

The eigenvalues, λ_{nm} , from Equation 5.77 are solutions to the first order differential equation given in Equation 5.78 [143].

$$\lambda J_n'(\lambda r_0) + h J_n(\lambda r_0) = 0 \tag{5.78}$$

Eigenfunctions, f_{nm} , for λ_{nm} from Equations 5.76–5.77 are given as

$$f_{nm}(r,\theta) = G_{nm}J_n(\lambda_{nm}r)cos(n\theta)$$
(5.79)

with G_{nm} defined as

$$G_{nm} = \frac{\lambda_{nm}^2}{\pi (h^2 r_0^2 + \lambda_{nm}^2 r_0^2 - n^2) J_n^2(\lambda_{nm} r_0)}$$
(5.80)

The functions, U_{1nm} , from Equations 5.76–5.77 [143] are given as

$$U_{1nm} = \frac{1}{\lambda_{nm}^2 + b^2} \int_0^{r_0} \int_0^{2\pi} a_1(r,\theta) f_{nm}(r,\theta) \ r \ dr \ d\theta$$
(5.81)

5.3.2.2 Numerical simulation

The numerical approach to computing the thermal response of the irradiated cylinder from [143] proceeds with the mathematical discretization of the bio-heat equation from Section 5.2.2. A discretized 2D model of the cylinder's cross sectional area is considered, as in Figure 5.11. The implementation of the numerical method is formulated using Equations 5.54–5.55. Initial temperature distribution is first computed in the absence of electromagnetic exposure. Subsequently, the computed SAR is introduced in order to calculate the thermal increase above the initial distribution.



Figure 5.11: 2D model space of the irradiated cylinder excluding PML boundaries

5.3.2.3 Comparison at 2.45GHz irradiation

The parameters used to compute the thermal response of the cylinder to the 2.45GHz plane wave are summarized in Table 5.4 [143]. The comparison of the analytically computed response to the numerically computed response is plotted in Figure 5.12a. The same cylinder model with 100 cells across the radius corresponding to a radius of $r_0 = 0.05$ m is used. As with the SAR comparisons, the analytical solution is represented by the continuous curve plotted as a function of the wave penetration depth into the cylinder with the overlayed discrete points representing the predicted temperature from the numerical method taken at cells along the cylinder diameter perpendicular to the plane wave. Clearly, heating occurs near the irradiated side of the cylinder where the SAR is concentrated. The region of the cylinder opposite of the plane wave remains close to the initial temperature, since the SAR at 2.45GHz does not penetrate to this depth. A color-mapped two dimensional cross section of the thermal response obtained from the numerical method using the SAR at 2.45GHz from Figure 5.9b is provided in Figure 5.12b.

Symbol	Physical Property	Value	Units
ρ	mass density	1070	$\left[\frac{kg}{m^3}\right]$
C	specific heat	3140	$\left[\frac{J}{kg^{\circ}C}\right]$
K	thermal conductivity	0.502	$\left[\frac{J}{m \ s^{\circ} C}\right]$
H	convective transfer constant	8.37	$\left[\frac{J}{m^2 \circ C}\right]$
	(for environmental ambient temperature)		1111 0 0 1
A_0	basal metabolic rate	1005	$\left[\frac{J}{m^3s}\right]$
В	blood perfusion constant	1674	$\left[\frac{m}{m^3 s^{\circ} C}\right]$
T_a	fixed environmental ambient temperature	24	°C
T_b	fixed blood temperature	37	$^{\circ}\mathrm{C}$
δx	Resolution of the cylinder model	0.5	mm
I_{max}	Number of rows in the 2D model space	220	_
J_{max}	Number of columns in the 2D model space	220	_

Table 5.4: Parameters for the thermal validation at 2.45GHz



(b) Numerical temperature distribution

Figure 5.12: Temperature distribution in the test cylinder at 2.45GHz irradiation

5.3.2.4 Comparison at 2MHz irradiation

A similar comparison between the analytical and numerical thermal solutions is conducted for the case of a 2MHz plane wave irradiating the cylinder model. The parameters which are used to compute the thermal response at 2MHz are summarized in Table 5.5. Note that the temperature distribution here tends to track the SAR distribution as lower conductivity and longer wavelength at 2MHz yields a SAR with greater penetration depth. A color-mapped two dimensional cross section of the thermal response obtained from the numerical method using the SAR at 2MHz from Figure 5.10b is provided in Figure 5.13b.

Symbol	Physical Property	Value	Units
ρ	mass density	1070	$\left[\frac{kg}{m^3}\right]$
C	specific heat	3140	$\left[\frac{J}{kg^{\circ}C}\right]$
K	thermal conductivity	0.502	$\left[\frac{J}{m \ s^{\circ}C}\right]$
H	convective transfer constant	8.37	$\left[\frac{m}{m^2 s^{\circ} C}\right]$
	(for environmental ambient temperature)		
A_0	basal metabolic rate	1005	$\left[\frac{J}{m^3s}\right]$
B	blood perfusion constant	1674	$\left[\frac{mJ}{m^3s^{\circ}C}\right]$
T_a	fixed environmentalal ambient temperature	24	°C
T_b	fixed blood temperature	37	$^{\circ}\mathrm{C}$
δx	Resolution of the cylinder model	0.5	mm
I_{max}	Number of rows in the 2D model space	220	—
J_{max}	Number of columns in the 2D model space	220	_

 Table 5.5: Parameters for the thermal validation at 2MHz



(a) Analytical versus numerical temperature



(b) Numerical temperature distribution

Figure 5.13: Temperature distribution in the test cylinder at 2MHz irradiation

The slight differences between analytical and computed results observed at the frequency of 2MHz are likely due to the course resolution used to model the cylinder at 2MHz in order minimize the simulation length. These comparisons indicate that the numerical methods for computing SAR and thermal distributions track their analytical counterparts reasonably well, down to 2MHz where studies of the retinal prosthesis are conducted.

5.4 Model generation

5.4.1 Development of a detailed 2D human eyeball model

Whereas the analytical methods for the calculation of SAR and temperature distributions are restricted to simple geometries such as cylinders and spheres, the numerical methods can address most structures of non-homogeneous composition. This section summarizes the development of a human eye model suitable for performing electromagnetic and thermal simulations to study temperature rise resulting from inductive coupling to the implant and intraocular operation of the implant itself. A number of eye models exists which take into account the most prominent eye features, including sclera, cornea, and lens [122], [144]. In this study, temperature elevation in the eye and surrounding head tissues due to the prosthesis is of interest, particularly near the retina. Therefore, a model is developed here which includes additional anatomical features, including the retina, and the cooling influence of choroidal blood flow.

The model is derived from the sketch of a human eye [145], [146], which was electronically scanned to obtain an image of roughly 600×600 pixel resolution. Subsequently, the muscles connecting to the sclera and the optic nerve were removed. The resulting image was then color segmented according to the distinct tissues represented, as shown in Figure 5.14.



Figure 5.14: Color segmentation according to tissue type

A software application has been developed (Figure 5.15) to discretize the segmented eye image onto a uniform grid of chosen resolution in order to sample it to a high resolution for construction of the model. At each cell in the overlying grid, the discretizer determines the dominant tissue type occupying that cell and identifies it according to the applied color segmentation. A unique tissue identifier is assigned to each cell location which is used as an index into a table of tissues (see Table 5.6) specifying dielectric and thermal properties. The resulting eye model which has been discretized to a spatial resolution of 0.25mm is shown in Figure 5.16.



Figure 5.15: Sampling software for spatial discretization of the human eye onto a uniform grid

5.4.2 Development of a detailed 2D human head model

In developing a model of the human eye for the electromagnetic and thermal simulations, tissues surrounding the eye will be influential in determining the steady state SAR and temperature distributions. Therefore, a combined head/eye model is sought, rather that simulating the eye in isolation from the head. A new two dimensional head model was constructed with a resolution of 0.25mm suitable for an accurate representation of the finest anatomical details of the human head and eye.

The National Library of Medicine and several other organizations have published data sets of the Visible Man Project [147]. This endeavor consists of encasing a human



Figure 5.16: 2D eye model sampled to 0.25mm spatial resolution using a uniform grid

male/female cadaver length-wise in a polymer. The body is then progressively sliced completely across the major axis at uniform stepping resolution (1mm, for example) while a camera oriented toward the cutting plane photographs the exposed slices. This is performed for the entire body to obtain a database of slices that can be rendered to produce slice imagery parallel not only to the slicing plane (axial orientation), but also in the two orthogonal planes perpendicular to the slicing plane (coronal and sagittal orientations). A sample slice taken at the position of the eyes is provided in Figure 5.17 [148] with tissue annotations also defined in [148].



Figure 5.17: Annotated photograph of a 2D human head slice taken from the *Visible* Man Project

As was done in constructing the 0.25mm eye model, derivation of the head model from Figure 5.17 proceeds by first color segmenting the head in order that tissues may be identified by uniform color. Subsequently, the discretizer software is again used to sample the head slice image to a 0.25mm model as shown in Figure 5.18, with a resulting tissue identifier assigned to each grid cell corresponding to an index into the table of dielectric and thermal properties for the tissues (see Table 5.6). The resulting head model at 0.25 mm is shown in Figure 5.19.

5.4.3 Merging the head and eye models

With 0.25mm head and eye models available as shown in Figure 5.16 and Figure 5.19, respectively, it remains only to combine these in order to arrive at a model suitable


Figure 5.18: Sampling software for spatial discretization of the human eye to a uniform grid

for numerical simulations for the retinal prosthesis. The combined model is shown in Figure 5.20. It is expected that temperature increases arising from inductive coupling and from the active micro-stimulator implant will be localized to the region of the eye. Therefore, in order to decrease the required memory and simulation time, the head/eye model of Figure 5.20 is truncated posterior to the eyes as shown in Figure 5.21. When computing specific absorption rate, this reduced model is overlapped along the posterior edge and surrounded along the remaining sides with the perfectly matched layer in order to correctly support the model truncation. Regarding heat, thermal conduction occurs in the interior region of the model, while at the anterior



Figure 5.19: Color segmentation of the human head slice photograph of Figure 5.17

boundary between the head and the surrounding environmental ambient, the convective boundary condition is applied. Since, the posterior boundary does not represent a "real" interface to the surrounding environmental ambient, convection is not applied at this edge. Rather, the initial steady state temperature distribution which was computed in the absence of any SAR and implant heating is forced along the posterior boundary in order to prevent inappropriate heat exchange with the surroundings. Once again, the model truncation was chosen at a distance to which the conduction of internal heat is expected to be negligible.



Figure 5.20: Merged model of the discretized head and eye models

5.4.4 Physical properties of tissues

The dielectric properties for the bodily tissues constituting the spatially discretized head/eye models have been collected from the *Dielectric Properties of Body Tissues* online database [149]. This data is compiled and organized by the *Electromagnetic Wave Research Institute* of the *Italian National Research Council* (IROE-CNR), based on work of researchers at *Brooks Air Force Base* [150], [151] dating back to 1996. The permittivities and conductivities are evaluated at 2Mhz corresponding to the carrier frequency of the exterior transmitter coil in the inductive telemetry



Figure 5.21: Truncated model of the merged human/eye models with inclusion of the silicon stimulator IC model in the left eye

scheme. Thermal properties and specific gravities for the biological tissues have been gathered primarily from [152] released in 1990, but also from the electromagnetic exposure studies of other researchers [122], [127]–[129], who cite sources [133] and [153]–[159], dating back to 1961. The *Retina-3.5* stimulator IC fabricated in bulk CMOS, is uniformly modeled with the physical properties of intrinsic silicon available from the online elemental database [160] dating to 1993.

5.4.5 Model and tissue property assumptions

As there is no single source for the thermal properties of the tissues comprising the head and eye models, the values have been taken from various publications collectively representing the research in electromagnetic and thermal dosimetry. Furthermore, values for some of the tissues are not explicitly available and in this case, values have been taken which match with tissues of nearest expected composition or water content. These are summarized as follows and also in the footnotes of Table 5.6.

In regards to the eye's anatomical detail, the model accounts for sclera, cornea, aqueous humor, pupillary sphincter muscle, the posterior chamber, the crystalline

Tissue	Relative	Conduct-	Mass	Specific	Thermal	Blood	Metabolic
	Permittivity	ivity	Density	Heat	Conductivity	Perfusion	Rate (Basal)
	ϵ_R	$\sigma\left[\frac{S}{m}\right]$	$\rho \left[\frac{kg}{m^3}\right]$	C $\left[\frac{J}{kg \circ C}\right]$	K $\left[\frac{J}{m \ s \ ^{\circ}C}\right]$	$\mathbf{B}\left[\frac{J}{m^3 \ s \ ^\circ C}\right]$	$A_0\left[\frac{J}{m^3 s}\right]$
air	1.000	0.0000	1.16	1300	0.250	0	0
muscle	826.000	0.5476	1040	3600^{-20}	$0.498 \ ^{12}$	2700	690
deep fat	22.950	0.0255	920	2500^{-20}	0.250^{-13}	520	180
bone	106.000 ⁴	0.0285 ⁴	1810	1300 ⁸	0.300^{-14}	1000	0
cartilage	815.500	0.2776	1100	3400^{-20}	0.450^{-20}	9100	1000
skin	858.000	0.0371	1010	3500^{-20}	0.420^{-20}	9100	1000
nerve	554.800	0.1556	1043 ⁹	3600 ⁹	0.503^{-9}	35000^{-9}	10000 ⁹
subcutaneous fat	22.950	0.0255	920	2500	0.250	520	180
brain grey matter	656.500	0.1807	1039 18	3680 ¹⁸	0.565^{-18}	35000	10000
brain white matter	340.600	0.1118	$1043 \ ^{18}$	3600 ¹⁸	0.503 18	35000	10000
blood	1681.000	0.9261	1060	$3840 \ ^{10}$	0.530^{-15}	_	0
sclera	1145.000	0.6889	1170	4178 11	$0.580 \ ^{11}$	0	0
scleral muscle ⁶	826.000 ⁶	0.5476^{-6}	1040^{-6}	3430^{-6}	0.498^{-6}	2700^{-6}	690 ⁶
cornea	1429.000	0.7438	1076 ¹⁸	4178 11	$0.580 \ ^{11}$	0	0
pupillary muscle ⁶	826.000^{-6}	0.5476^{-6}	1040^{-6}	3430^{-6}	0.498^{-6}	2700^{-6}	690^{-6}
post chamber 5	76.650 5	1.5010 ⁵	$1003 \ {}^{5}$	$3997 \ {}^5$	0.578 5	0^{5}	0^{5}
lens	829.700	0.4170	1100	3000 11	0.400^{-11}	0	0
lens zonules ⁶	826.000^{-6}	0.5476^{-6}	1040^{-6}	3430^{-6}	0.498^{-6}	2700^{-6}	690^{-6}
cilliary muscle ⁶	826.000^{-6}	0.5476^{-6}	1040^{-6}	3430^{-6}	0.498^{-6}	2700^{-6}	690^{-6}
aqueous humor	76.650 ¹⁷	1.5010 ¹⁷	$1003 \ ^{18}$	$3997 \ ^{19}$	0.578 18	0	0
vitreous humor	76.650	1.5010	1009 18	$3997 \ ^{19}$	0.594 ¹⁸	0	0
choroid ⁷	1681.000 ⁷	0.9261 ⁷	1060 7	3840 ⁷	0.530^{-7}	0 7	0 7
retina	1145.000	0.6889	$1039 \ ^{16}$	$3680 \ ^{16}$	$0.565 \ ^{16}$	$35000 \ ^{16}$	$10000 \ ^{16}$
silicon	-21	- ²¹	2330 ²²	959 ²²	150.000 ²³	—	—

Table 5.6: Dielectric and thermal properties of tissues and materials in the head/eye model at $2MHz^{1,2,3}$

¹Dielectric properties, ϵ_R and σ , are taken from [149] unless otherwise noted

 $^2 \rm Mass$ density, $\rho,$ taken from [129] unless otherwise noted

³Blood perfusion constant, B, and basal metabolic rate, A_0 , are taken from [128] unless otherwise noted

⁴Cortical bone, taken from [149]

⁵Unavailable explicitly. Therefore, assigned the properties of aqueous humor

⁶Taken as muscle (generic)

⁷Modeled as blood

⁸Human cortical bone, taken from [152]

⁹Unavailable explicitly. Therefore, assigned the properties of brain white matter, as this is reported to have a high nerve fiber makeup and is contained in the optic nerves [124]

¹⁰Human whole blood

¹¹Taken from [122]

¹²Human skeletal muscle, taken from [152]

¹³Averaged human subcutaneous fat, taken

from [152]

¹⁴Taken from [127]

¹⁵Human whole blood (43% Hct), taken from [152]

¹⁶Unavailable explicitly. Therefore, assigned the properties of brain grey matter, as this is reported to have a higher concentration of neural cell bodies and dendrites than white matter [124]

¹⁷Unavailable explicitly. Therefore, assigned the properties of Vitreous Humor

¹⁸Taken from [152]

¹⁹Taken as Humor from [122]

 20 Taken from [128]

 21 Silicon not used in the calculation of the specific absorption rate

 22 Taken from [160]

²³The thermal conductivity of the implant is dependent on the precise material composition of the stimulator IC, any additional supporting intraocular components, and the hermeticallysealed biocompatible casing. Therefore, thermal simulations were conducted with values of $K_{chip} \in \{10, 20, 30, ..., 80, 90\}$ $\left[\frac{J}{m \ s \ c}C\right]$, so as to characterize the dependence of temperature increase on the chip's thermal conductivity. Subsequently, in order to minimize the computational time, temperature rise associated with $K_{SI} = 150$ (corresponding to the real value of silicon) is extrapolated according to the resulting trend. lens, the lens zonules, the cilliary muscle, vitreous humor, the choroid, and the retina. Although this accounts for eleven tissue types in the eye model, explicit physical properties for all of these have not been located in the literature, as they have not been considered "major" tissues in head models of dosimetry studies to date [122], [127]-[129]. Nonetheless, unique identifiers are maintained for these ocular tissues such that the model can be updated through Table 5.6 as supporting physical properties become available. In the interim, the pupillary and cilliary muscles, the lens zonules (likened to tendons), and the muscles attached to the sclera are represented with the dielectric and thermal properties of generic human muscle. Due to its close proximity, the posterior chamber situated between the lens and pupillary muscle takes its properties from the aqueous humor. Since [149] provides properties for vitreous humor and not aqueous humor, the permittivity and conductivity of the aqueous humor at 2MHz are taken as vitreous. Similarly, the mass density and thermal conductivity are shared among the aqueous and vitreous as |152| identify a single humor for these two properties. Moreover, the specific heat properties are equal, as [122] also identifies a single humor. The highly vascularized choroid which lies between the sclera and retina and nutriates the outer retina, is approximated with the physical properties of blood.

As it relates to the retina, only the dielectric properties have been found in available research literature [149]. Mass density and thermal properties have not been explicitly located. The retina is a multilayer neural structure approximately 300μ m thick with most of its composition organized as a cascade of various neuron cell types and their interconnections [52], [145], [161], [162]. Only in the innermost layer above the ganglion neurons is there a heavily axonal or nerve fiber layer. Therefore, in its composition, the retina is expected for the greater part to be analogous to brain grey matter, where there is a higher concentration of neural cell bodies and dendrites [124]. Therefore, the mass density and thermal properties of retina in Table 5.6 follow those of brain grey matter.

White matter represents the portion of brain neural structure involved in communication between areas of grey matter and thus has a high nerve fiber, or axonal, composition [124]. Furthermore, as the optic nerves are reported to contain white matter [124], physical properties of nerve are assumed similar to those of white matter. Moreover, [128] and [163] report blood perfusion and basal metabolism in agreement with that of brain, or white matter. Hence, physical properties for nerve in Table 5.6 are assigned from those explicitly available for brain white matter.

The thermal conductivity for the uniform silicon model of the *Retina-3.5* stimulator IC was reported in [160] as 150 $\left[\frac{J}{m \ s \ \circ C}\right]$, which exceeds thermal conductivities of the biological tissues by two order of magnitude. In accordance with Equation 5.54, this yields a much longer simulation when compared with the case where silicon is absent from the model. It was expected that a lower assumed thermal conductivity for silicon would not strongly invalidate thermal predictions while still improving simulation time. The thermal conductivity of the implant is dependent on the precise material composition of the stimulator IC, any additional supporting intraocular components, and the hermetically-sealed biocompatible casing. Therefore, thermal simulations were conducted with values of $K_{chip} \in \{10, 20, 30, ..., 80, 90\}$ $\left[\frac{J}{m \ s \ c}C\right]$, so as to characterize the dependence of temperature increase on the chip's thermal conductivity. Subsequently, in order to minimize the computational time, temperature rise associated with $K_{SI} = 150$ (corresponding to the real value of silicon) is extrapolated according to the resulting trend.

5.5 Scaling consideration from 3D to 2D

5.5.1 Modeling the extraocular power/transmitter coil

As the simulations of temperature increase in the head/eye model developed here are conducted in two dimensions, special treatment is required for the transmitter coil. The current version of the telemetry system includes an extraocular transmitting multi-turn coil of diameter two inches located at a distance of approximately 2cm from the human eye, and an intraocular receiving multi-turn coil of diameter 7mm that replaces the crystalline lens. In typical usage of the *Retina-3.5* stimulator IC in which it is assumed that the implant is operating with all channels active at current levels 50% of maximum specifications, required continuous supply currents of 10mA were determined. Experiments with inductive coupling based on the work reported in [78] showed that a power of 200Vpp and 2A at 2MHz in the transmitting coil was necessary to obtain 10mA of supply current at $V_{dd}=5V_{DC}$ and $V_{ss}=-5V_{DC}$ derived from the receiving coil.

For a low-frequency three dimensional coil of radius, R, and turns count, N, carrying a current of I, the magnetic field, $\vec{\mathbf{H}}$, is given in Equation 5.82 [164].

$$\|\vec{\mathbf{H}}\| = \frac{NI}{2R} \tag{5.82}$$

The coil current in a three dimensional model space would be approximated with a finite number of tangential current vectors positioned around the circumference of the coil as illustrated in Figure 5.22a. However, for performing two dimensional simulations, the coil current is represented with two parallel and tangential current vectors of opposite polarity as in Figure 5.22b.

However, this approximation does not produce electric and magnetic fields with the same distributions as in the three dimensional case as can be seen in Figure 5.23a



Figure 5.22: Scaling considerations between 3D and 2D

for the three dimensional coil of Figure 5.22a and in Figure 5.23b for the two dimensional coil of Figure 5.22b. Results are shown in dB to enhance the differences. These distributions were obtained using analytical methods explained in [165] applied to the two and three dimensional radiating structures of Figure 5.22 for for 2A coil current and frequency of 2Mhz, while corrsponding FDTD simulations produced identical results.

To compensate for the differences in the two distributions, the resulting fields for the two dimensional coil are scaled such that the value of $\vec{\mathbf{H}}$ evaluated at the center of the multi-turn external coil in the 2D sense matches the theoretical value from Equation 5.82, which would result from simulations involving a three dimensional coil model.

The distributions of Figures 5.23 also show that the two and three dimensional cases are characterized by different rates of decay of the electromagnetic field. As

such, it has been verified that, given the coil dimensions and its distance from the surface of the eye, the two dimensional field approximation closely parallels the three dimensional one within the eye region. Furthermore, it has been verified both numerically and analytically [165] that the two dimensional equivalent coil represents the worst-case scenario, in the sense that the fields induced in the eye and head computed by the two dimensional radiating model are generally higher than the corresponding fields computed by the three dimensional model.



Figure 5.23: Electric field distributions for 2D and 3D coil structures

5.5.2 Modeling power dissipation in the stimulator microchip

Modeling of the stimulator microchip also requires approximations that allow us to correctly represent the power dissipated by the chip in a two dimensional space, rather than three dimensional. MOSIS reports the die size for the *Retina-3.5* stimulator IC in the AMI-1.2 μ m process as 4.7mm×4.6mm×500 μ m. However, after accounting for clearance around the pad-ring for the wafer dicing saw, the actual die size becomes 5.53mm×5.25mm×508 μ m. Discretizing this chip volume to 0.25mm spatial resolution, yields the 3D chip model shown in Figure 5.24a with cellular dimensions $I = 22 \times J = 21 \times K = 2$, with the total power dissipation expressed as a volume summation of the discrete power density, $P_{chip(3D)}^{(density)}(i, j, k)$, as given in Equation 5.83. (discrete)



Figure 5.24: *Retina-3.5* stimulator IC models discretized to 0.25mm uniform spatial resolution

$$P_{chip(3D)} = \sum_{i=1}^{I} \sum_{j=1}^{J} \sum_{k=1}^{K} P_{chip(3D)}^{(density)}(i, j, k)$$
(5.83)

When considering a 2D model of the 3D stimulator chip for thermal simulation in the 2D head/eye model of Figure 5.21, the total power, $P_{chip(3D)}$, is retained by integrating (or summing) the power density for the 3D chip model along the *k*-axis for each cell (i, j) in the 2D chip model. Although this yields power density units in 2D of $\left[\frac{W}{m^2}\right]$ it is considered that the 2D model shown in Figure 5.24b can be conceptually extended infinitely in the k-dimension. Therefore units of $\left[\frac{W}{m^3}\right]$ are retained in the 2D chip model for the power density at (i, j) consistent with the units of the tissue properties, such as mass density ρ in $\left[\frac{kg}{m^3}\right]$. This means of condensing the power density is formulated as:

$$P_{\substack{chip(2D)\\(\underline{discrete})}}^{(density)}(i,j) = \sum_{k=1}^{K} P_{\substack{chip(3D)\\(\underline{discrete})}}^{(density)}(i,j,k)$$
(5.84)

In general the power density varies across a chip, but in the case of the *Retina-3.5* stimulator, the IC consists of an array of 60 identical stimulus current driver circuits which are uniformly distributed over 75% of the chip area (25% is occupied by digital control circuits). Thus, the power density is approximated as uniformly distributed, such that

$$P_{\substack{chip(2D)\\(\underline{discrete})}}^{(density)}(i,j) = \sum_{k=1}^{K} \frac{P_{chip(3D)}}{(I\,dx)(J\,dy)(K\,dz)},$$
(5.85)

where dx = dy = dz = 0.25mm, and I = 22, J = 21, and K = 2. The power density, $P_{chip(2D)}^{(density)}(i, j)$, as defined here and associated with the 2D chip model of Figure 5.24b, (discrete) is the same value used in the 2D bio-heat formulation of Equation 5.55.

5.6 Results

As is indicated in Equation 5.44, the specific absorption rate and the dissipated stimulator IC power are the mechanisms for temperature increase which are expected to account for some ocular heating. Therefore, the numerical FDTD method for specific absorption rate summarized in Section 5.2.1 and the numerical thermal method summarized in Section 5.2.2 are applied to the head/eye model of Figure 5.21 to estimate the increase in temperature. In order to gain further insight into the results, the influence of SAR and dissipated power in the implant are considered separately.

5.6.1 Specific absorption rate

Recall that experiments with inductive coupling based on the work reported in [78] showed that a power of 200Vpp at 2A in the primary coil was necessary to obtain 10mA of source current at $V_{dd}=5V_{DC}$ and $V_{ss}=-5V_{DC}$ on the secondary side (power receiving coil). Therefore, the specific absorption rate distribution resulting from the numerical FDTD at 2MHz has been linearly scaled to reflect the primary side input power used in these experiments. A color-mapped graphical representation of the resulting SAR is provided in Figure 5.25. The primary coil was considered with a 2-inch diameter and 10 turns. In two dimensions, it is represented as two point sources of opposite polarity. The coil is positioned as indicated in Figure 5.25 above the left eye at a location consistent with attachment to a pair of framed reading glasses.



Figure 5.25: Specific absorption rate in log scale at 2MHz irradiation for two amps of coil current

Power levels are scaled to $\left[\frac{mW}{kg}\right]$ and are provided in \log_{10} scale for best viewing

and in the normal linear scale. Note that there is a clear delineation along the axis of the coil passing through the center of the left eye. This marks the locus of points where the magnetic field is maximum and the electric field is minimum. The electric field increases away from this axis. The SAR distribution shows that the right eye receives more deposited power than the targeted left eye containing the prosthesis. The major reason for the location of this peak SAR in the right eye is the much higher conductivity of the eye humor with respect to other organs, such as cartilage, bone, or skin. The left eye with the prosthesis is exposed to minimal electric field (electric field on the axis of the coil is ideally zero) while the largest electric field is found on the sides of the coil. Thus, the opposite eye is exposed to large electric fields compared to organs normal to the axis of the coil and, considering the higher conductivity of the eye humor, this results in relatively high SAR compared to other organs. Since losses are associated with the electric field $\left(ie - \text{recall}, \text{SAR} = \frac{\sigma ||\vec{\mathbf{E}}||^2}{2\rho}\right)$, the results show that the right eye receives more deposited power that the targeted left eye.

5.6.2 The influence of choroidal blood flow on ocular temperature

Studies have revealed a relationship between damage to the photoreceptor layer of the retina and ocular temperature [166], [167]. Posterior to the human retina's photoreceptor layer and to the pigmented epithelium lies the choroid which is a vascularized layer supplying blood to the outer retina. The blood circulation density to the outer retina by way of the choroid is known to be higher than in any other bodily tissue [168], [169]. In fact, the blood flow exceeds the oxygenation needs of the outer retina and the retinal pigment epithelium [168], [169]. It is proposed that the high blood flow from the choroidal layer facilitates the regulation of retinal temperature which would otherwise increase in the outer retina during the photo-transduction of incident light and absorption in the epithelium of excess light energy [170]. Experiments

revealed that less energy from incident light was necessary in dead animals than in living animals to incur retinal damage [168]. Furthermore, reducing blood flow in living animals also encouraged retinal damage from light energy. Other studies revealed a type of closed loop neural feedback in which increased energy from incident light produced an increase in choroidal blood flow [171], [172].

In order to gain insight into the influence of choroidal blood flow on ocular cooling, numerical simulations are conducted to compare thermal results first assuming no choroidal blood flow in the head/eye model of Figure 5.21 and subsequently with blood flow modeled. Under both assumptions, the choroid is not considered equivalent to blood, but is instead identified as an independent, unique tissue type. However, because it is heavily vascularized, it is modeled with the same dielectric and thermal properties and mass density of blood.

In Section 5.6.3, the absence of choroidal blood flow is considered with numerical thermal predictions provided given this assumption. Accordingly, the temperature of the choroidal tissue is allowed to rise as dictated by the bio-heat equation, as any other tissue type would when exposed to heat. Note that the retina is assigned a high blood perfusion constant in Table 5.6, wherein the source of this blood is the adjacent choroidal tissue. Thus, the additional constraint is imposed that the parameter of T_b occurring in the bio-heat equation when evaluating retinal temperature will be assigned from the computed variable temperature of the choroid, and will not be considered fixed at 37°C as is the case for other tissues. This is best reconciled by considering a fixed parameter $T_b=37^{\circ}$ C for all perfused tissues except retina and a variable parameter $T_{choroid} \neq T_b$. Thus, the cooling term in the bio-heat equation would be $-B(T - T_b)$ for non-retinal tissue and $-B_{retina}(T_{retina} - T_{choroid})$ for retina.

In Section 5.6.4, the presence of choroidal blood flow and its impact of regulating retinal temperature is considered, again from the perspective of numerical thermal simulation. Since, the choroidal blood flow rate is unknown and is also considered to vary with incident light energy [171], [172], the heat dissipating influence of flowing blood is modeled by holding the choroidal temperature at $T_b = 37^{\circ}$ C, thereby assuming ideally an "infinite" blood flow. In the biological system, the blood is expected to increase above $T_b = 37^{\circ}$ C as it carries away heat absorbed in the outer retina and pigmented epithelium. But as it immediately flows away and is replaced by fresh blood, a fixed choroidal temperature of $T_{choroid}=T_b=37^{\circ}$ C in the head/eye model of Figure 5.21 is assumed to closely approximate the true response of the choroid. Thus, for the simulations results of Section 5.6.4, an infinite blood flow characterized by $T_{choroid}=T_b=37^{\circ}$ C is assumed.

5.6.3 Thermal simulations in the absence of choroidal blood flow

5.6.3.1 Initial temperature distribution

Since the thermal elevation **above** the natural temperature distribution is of interest, it is necessary to simulate the heating distribution in the head/eye model of Figure 5.20 beginning at an initial assumed environmental ambient temperature of 24°C, while devoid of the influence of SAR and of power dissipation in the stimulator IC. This and the subsequent thermal simulations using the model of Figure 5.20 assume the thermal properties of Table 5.6. The results of this simulation are presented in Figure 5.26 and appear consistent with expectations of the natural temperature distribution in the human head. A peak temperature of 37.2857°C occurs within brain due to the high basal metabolism associated with white and grey matter as seen in Table 5.6. Cooler temperatures occur near the interface between the head model and the surrounding environmental ambient where thermal convection occurs.



Figure 5.26: Computed initial temperature distribution in the human head/eye model in the absence of choroidal blood flow and with no excitation from SAR or from power dissipation in the stimulator IC

The anterior portion of the initial temperature distribution corresponding to the truncated head/eye model of Figure 5.21 is isolated from Figure 5.26 as shown in Figure 5.27. This is used to initialize the thermal simulations of SAR and of the implant IC in the absence of blood flow in the choroid. A peak temperature of 37.1094°C occurs in anterior portion of the initial temperature distribution, again associated with the brain owing to high basal metabolism.



Initial temperature distribution in the human head/eye model

Figure 5.27: Computed initial temperature distribution (anterior portion) in the human head/eye model in the absence of choroidal blood flow and with no excitation from SAR or from power dissipation in the stimulator IC

5.6.3.2 Temperature increase due to SAR

As indicated in Section 5.4.3, because the increase in temperature resulting from both SAR and the implant IC is not expected to impact the entire head, only the anterior portion of the head is used in order to further decrease simulation time. Again, thermal conduction is applied to the interior region of the model, while at the anterior boundary between the head and the surrounding ambient, the convective boundary condition is applied. Along the artificial interface to the surrounding ambient environment at the truncating edge, the initial steady state temperature distribution from Figure 5.26 is applied, in order to prevent inappropriate head exchange with the surroundings. Once again, the model truncation was chosen at a distance to which the conduction of internal heat is expected to be negligible.

The head/eye model of Figure 5.21 includes a uniform silicon model of the stimulator IC positioned at mid-vitreous in the left eye. In order to study temperature increase due to SAR separately, the presence and influence of the stimulator IC are set aside for independent thermal simulations. Therefore, the power dissipation associated with the stimulator IC is temporarily set to zero. The silicon IC model is also temporarily removed and replaced with vitreous humor such that left and right eye models are identical.

A thermal simulation predicting the temperature increase arising from the SAR of Figure 5.25 is run with a simulated time coverage of one hour. At the end of one hour of simulated time, the peak temperature rise in the right eye has converged to a value of 0.0685° C and the rate of increase has diminished to approximately $10^{-6} {}^{\circ}$ C when monitored at 0.5s intervals. The thermal results are summarized in Table 5.7 for each eye from the model of Figure 5.21.

A plot of temperature increase over time due to SAR for the left and right eyes is provided in Figure 5.28. The vertical axis represents the temperature increase

[Model region ¹	Maximum	Maximum	Peak increase	Elapsed
		SAR	$temperature^2$	above initial	time
				$temperature^{3}$	
			Т	$\Delta T = T - T_0$	t
		$\frac{\text{mW}}{\text{m}^3}$	$[^{\circ}C]$	$[^{\circ}C]$	[minutes]
	over left eye	111.9966	36.8218	0.0079	60
	over right eye	404.1180	36.8189	0.0685	60

Table 5.7: Temperature elevations resulting from the thermal simulation of SAR, corresponding to Figure 5.25, in the absence of choroidal blood flow

¹Corresponding to the head/eye model of Figure 5.21

²These predicted steady state temperatures in the left and right eyes remain less that the highest temperature, $T_{max} = 37.1094^{\circ}C$, from Figure 5.27 which is encountered in the brain tissue.

³These results represent the predicted steady state temperature increase in the left and right eyes between the initial and final temperature distributions

above the initial temperature distribution encountered over each eye. Recall that the SAR distribution of Figure 5.25 indicates most of the power is deposited in the right eye despite targeting the stimulator IC in the left eye, owing to the the $\vec{\mathbf{E}}$ -field distribution associated with the $\vec{\mathbf{H}}$ -field sourced from the primary coil. Accordingly, the peak thermal increase of 0.0685°C also occurs in the right eye. Note that the temperature rise in each eye asymptotically approaches steady state as heat continues to spread beyond the eyes and into the surrounding head tissues.

A color-mapped graphical plot of the temperature distribution resulting from the SAR of Figure 5.25 is provided in Figure 5.29. The predicted steady state temperature increase of 0.0685°C is indicated by the red area near the lens of the right eye. Once again, this is consistent with the location of the SAR maximum from Figure 5.25.

5.6.3.3 Sensitivity to implant material properties

The material composition of the implant directly influences it thermal properties, with particular emphasis here placed on the thermal conductivity. This represents a measure of how quickly accumulating heat propagates through the implant materials



Figure 5.28: Computed ocular heating versus time due to SAR in the absence of choroidal blood flow

and into the tissues of the head/eye model. Table 5.6 indicates that the thermal conductivities of the biological tissues varies only slightly around values of K=0.5 $\left[\frac{J}{m \ s \ c}C\right]$. In contrast, the microstimulator IC is composed mostly of silicon which asserts a thermal conductivity, $K_{SI}=150 \left[\frac{J}{m \ s \ c}C\right]$. Any additional materials used in the construction of the prosthesis may further increase the net thermal conductivity, particular metals. Thus, when examining the thermal response of the head/eye model to power dissipation in the microstimulator chip, the dependence of the numerical results on the thermal conductivity of the implant is considered. Recall from Section 5.2.2, that the maximum recommended time step to be taken in the numerical method is given by Equation 5.54. The presense and location of thermal conductivity, K_n , within this expression suggests that materials in the head/eye model which are of greater thermal conductivity force a smaller time step in the thermal method in order to ensure numerical stability. The trend is exponential and asserts so small a



Figure 5.29: Computed steady state ocular heating distribution due to SAR in the

absence of choroidal blood flow

time step when introducing $K_{chip} = K_{SI} = 150 \left[\frac{J}{m \ s \ \circ C}\right]$ that simulations of the head/eye model of Figure 5.21 become impractical, requiring a month or more to complete. ¹ Therefore, the strategy adopted here is to numerically simulate the thermal response of the head/eye model to power dissipation in the stimulator IC over several values of $K_{chip} K_{SI}$ in order to capture the relationship between steady state temperature increase and thermal conductivity. Following this, the thermal elevation for $K_{chip} = K_{SI}$, the true value for silicon, can be extrapolated.

The value of K_{chip} is allowed to take on values in the set $\{10, 20, 30, ..., 80, 90\}$, while a separate numerical simulation is run to predict the thermal increase associated with each value. Each of these simulations is performed for a power dissipation of

Time: 01:00:00

¹Since the completion of this work based on the bio-heat equation from [122], an unconditionally stable D-H formulation of the FDTD algorithm has been developed and published [173]. This allows a spatial and temporal discretization of the bio-heat equation to be formulated which does not require an impractially small time step in order to remain stable when modeling materials with high thermal conductivities, such as silicon in this case.

 $P_{chip(3D)} = 46.4672$ mW, corresponding to the expected worst case operating conditions summarized in Table 3.2. The simulations also assume no blood flow in the choroid beyond the outer retina. A plot of the predicted steady state temperature increase over time for each $K_{chip} \in \{10, 20, 30, ..., 80, 90\} \left[\frac{J}{m \ s \ \circ C}\right]$ is given in Figure 5.30 where the stimulator microchip is positioned in the left eye.



Figure 5.30: Computed ocular heating versus time for several values of thermal conductivity, K_{chip} , of the stimulator IC. These thermal evelations are simulated in the absence of choroidal blood flow and for expected worst case power dissipation, $P_{chip(3D)} = 46.4672$ mW.

The thermal computations over each value of K_{chip} are conducted for 60 minutes of simulated time. Following these nine simulations, the highest recorded temperature increases are plotted versus K_{chip} as shown in Figure 5.31, in order to characterize the relationship to thermal conductivity.

Attempts to analytically fit a polynomial to this data resulted in curves which passed well through the points but did not capture the trend in the data for values



Figure 5.31: Computed ocular heating versus thermal conductivity, K_{chip} , of the stimulator IC in the absence of choroidal blood flow and for expected worst case power dissipation, $P_{chip(3D)} = 46.4672$ mW.

of $K_{chip} > 100 \left[\frac{J}{m \ s \ \circ C}\right]$. The fitted equations quickly went unbounded outside of the range of the sample points. Therefore, a software program, *xtrain*, was developed and used to iteratively train an artificial neural network to fit this data. The interface for this software is illustrated in Figure 5.32, with the neuron output characteristics shown in Figure 5.33.

The software is designed to train artificial neural networks with an arbitrary number of inputs and outputs and containing any number of hidden layers and hidden layer neurons via the generalized back-progagation training algorithm [174]. The network structure of Figure 5.34 was found to provide sufficient learning capability to map the thermal simulation data. The network accepts a single input which is the microchip thermal conductivity, K_{chip} , and provides a single output, T_{max} , as



Figure 5.32: *xtrain* artificial neural network software (network configuration view) developed to map the trend in the data of temperature evelation versus thermal conductivity, K_{chip} , of the stimulator IC.

an estimate of the corresponding predicted steady state temperature increase. Internally, the network contains four neurons in a single hidden layer and one second-stage neuron in the output layer.

Once trained on the nine data points, the network models the trend in the data as indicated by the blue curve in Figure 5.31. The network's weights and neural biases as assigned in Figure 5.34 which were iteratively derived in learning the mapping to this data are given in Equations 5.86 and 5.87, respectively. These are applicable to the neural output equations which are annotated on the network diagram of Figure 5.34. For $K_{chip} = 150 \left[\frac{J}{m \ s \ c}\right]$, the network estimates a predicted steady state temperature increase of 0.6123°C, associated with the expected worst case power dissipation of



Figure 5.33: *xtrain* artificial neural network software (neural output view) developed to map the trend in the data of temperature evelation versus thermal conductivity, K_{chip} , of the stimulator IC.

 $P_{chip(3D)} = 46.4672$ mW in the stimulator IC in the absense of choroidal blood flow.

$$\begin{bmatrix} w_1 \\ w_2 \\ w_3 \\ w_4 \\ w_5 \\ w_6 \\ w_7 \\ w_8 \end{bmatrix} = \begin{bmatrix} -0.4517209832339053 \\ 0.0668279172344458 \\ 0.0450303006980529 \\ 0.1394951172747662 \\ 4.5376746316442782 \\ -1.2491959618556294 \\ -0.9317482528537849 \\ -1.8471016497767201 \end{bmatrix}$$
(5.86)
$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \end{bmatrix} = \begin{bmatrix} 3.1494399852355466 \\ -2.2351021009212220 \\ -3.6738981805796844 \\ -1.8845317664575965 \\ 1.2566306000267369 \end{bmatrix}$$
(5.87)



Figure 5.34: The artificial neural network structure selected to map the trend in the data of temperature evelation versus thermal conductivity, K_{chip} , of the stimulator IC.

5.6.3.4 Temperature increase due to power dissipation in the implantable stimulator IC

The estimates from Table 3.2 acquired from *Hspice* simulation are used to represent power dissipation in the silicon stimulator IC model contained in the head/eye model of Figure 5.21. These values give rise to the power densities specified in the bio-heat formulations of Equations 5.44, 5.53, and 5.55 based on the derivations in Section 5.5.2. These power densities in turn are passed to the thermal numerical method developed in Section 5.2.2 in order to predict ocular heating associated with the stimulator IC. A separate thermal simulation has been conducted for each of the twelve stimulator operating conditions in which variations in parameters of the biphasic stimulus current pulses are programmed. The power dissipation associated with each case is recorded in Table 3.2. As with the simulations of temperature increase due to SAR, the initial temperature distribution of Figure 5.26 is assumed at the start of thermal simulation.

A plot of temperature increase in the left eye over time for the twelve operating conditions is provided in Figure 5.35. In order to reduce the simulation time, a reduced hypothetical value of $K_{chip}=10$ is used to compute these baseline curves. The vertical axis represents the peak increase above the initial temperature distribution for the left eye of Figure 5.21 in which the stimulator IC is modeled. These thermal elevations are unrealistically high owing to the reduced thermal conductivity, $K_{chip}=10$. However, these estimates are rescaled for $K_{chip}=K_{SI}=150$ (the real value) as shown in Figure 5.36, according to the trend modeled in Figure 5.31. Notice the asymptotic convergence of temperature rise in the left eye occurring for each power dissipation estimate from Table 3.2, as heat spreads beyond the confines of the eye.

A plot of the temperature increase in the left eye versus power dissipation in the stimulator IC is provided in Figure 5.37 for the twelve programmed operating conditions. Each data point represents the highest recorded temperature increase in Figure 5.35 acquired from numerical simulation for each of the twelve operating conditions. The solid line represents a least squares linear fit to the numerical data. The result indicates that the predicted steady state temperature increase is linearly dependent on the power consumption, provided that the thermal properties of the tissues remain constant. Simulations of exceedingly large stimulator IC power dissipation are expected to inevitably deviate from realistic results, since the thermal properties of the tissues would eventually undergo change in the presence elevated heat. This would lead to a non-linear dependence of predicted steady state temperature increase on stimulator IC power dissipation. A color-mapped graphical plot of the temperature distribution arising from operation of the stimulator IC is provided in Figure 5.39a, corresponding to the worst case value of $P_{chip(3D)} = 46.4672$ mW from Table 3.2. A predicted steady state temperature increase of 0.8588°C was computed over the region of the stimulator IC in the left eye for $K_{chip} = 90 \left[\frac{J}{m \ s \ c}C\right]$, which was the highest value of thermal conductivity simulated in reference to the results plotted in Figure 5.30. The predicted steady state temperature increase extrapolated to $K_{chip}=K_{SI}=150 \left[\frac{J}{m \ s \ c}C\right]$ is 0.6123°C as indicated on the revised colorbar in Figure 5.39b. At the surface of the retina, the extrapolation of the predicted steady state temperature increase appears to be near 0.2°C-0.25°C. The highest recorded thermal elevations associated with the results plotted in Figure 5.36 extrapolated to $K_{chip}=K_{SI}$ are summarized in Table 5.8.

Table 5.8: Temperature elevations resulting from the *Hspice* simulated power dissipation estimates, $P_{chip(3D)}$, of Table 3.2, in the absence of choroidal blood flow

V_{dd}, V_{ss}	current	frame	pulse	Simulated	Peak increase above		Elapsed
		rate	width	chip power ¹	initial temperature ^{2,3}		time
		r 1	337	D			
	A	$I = \overline{T}$	vv	$\Gamma_{chip(3D)}$	$\Delta I = I - I_0$ [°C]		L.
$[V_{DC}]$	$[\mu A]$	[Hz]	[ms]	[mW]			[minutes]
					$K_{SI} = 10^{-4}$	$K_{SI} = 150^{-5}$	
+5, -5	400	50	1	9.1862	1.5278	0.1210	60
+5, -5	400	50	2	15.1580	2.5211	0.1997	60
+5, -5	400	50	3	21.1874	3.5239	0.2792	60
+5, -5	400	60	1	10.4012	1.7299	0.1371	60
+5, -5	400	60	2	17.6018	2.9275	0.2319	60
+5, -5	400	60	3	24.8018	4.1250	0.3268	60
+7, -7	600	50	1	16.3216	2.7146	0.2151	60
+7, -7	600	50	2	27.8308	4.6288	0.3667	60
+7, -7	600	50	3	39.4527	6.5617	0.5198	60
+7, -7	600	60	1	18.7112	3.1120	0.2465	60
+7, -7	600	60	2	32.5892	5.4202	0.4294	60
+7, -7	600	60	3	46.4672	7.7283	0.6123	60

¹Duplicated from Table 3.2

 $^2\mathrm{Absolute}$ temperatures are omitted for brevity, as thermal increase above the initial distribution is the parameter of interest.

³These results indicate the predicted steady state temperature increase over the left eye between the initial and final temperature distributions encountered over the duration of the simulation.

⁴These thermal elevations are computed for microchip thermal conductivity, $K_{chip}=10 \left[\frac{J}{m \ s \ c}\right]$, according to the results plotted in Figure 5.35.

⁴These thermal elevations are K_{chip} extrapolated to silicon thermal conductivity, $K_{SI}=150 \left[\frac{J}{m \ s \ cC}\right]$, according to the trend depicted in Figure 5.31, based on the computed results from Figure 5.35, as shown in Figure 5.36.



Predicted heating in left eye due to stimulator implant

Figure 5.35: Computed ocular heating versus time due to power dissipation in the stimulator IC for thermal conductivity, $K_{chip}=10 \left[\frac{J}{m \ s \ \circ C}\right]$ (reduced value) simulated in the absence of choroidal blood flow



Figure 5.36: Predicted ocular heating versus time due to power dissipation in the stimulator IC for thermal conductivity, K_{chip} , extrapolated to silicon thermal conductivity, $K_{SI}=150 \left[\frac{J}{m \ s \ c}\right]$ (real value), while in the absence of choroidal blood flow



Figure 5.37: Computed ocular heating versus power dissipation in the stimulator IC for thermal conductivity, $K_{chip}=10 \left[\frac{J}{m \ s \ ^{\circ}C}\right]$ (reduced value) simulated in the absence of choroidal blood flow



Figure 5.38: Predicted ocular heating versus power dissipation in the stimulator IC for thermal conductivity, K_{chip} , extrapolated to silicon thermal conductivity, $K_{SI}=150 \left[\frac{J}{m s \circ C}\right]$ (real value), while in the absence of choroidal blood flow





(b) Rescaled colorbar for the distribution where microchip thermal conductivity, K_{chip} , is extrapolated to silicon thermal conductivity, $K_{SI}=150 \left(\frac{J}{m \ s \ \circ C}\right)$

Figure 5.39: Computed steady state ocular heating distribution due to expected worst case power dissipation, $P_{chip(3D)} = 46.4672$ mW, in the stimulator IC in the absence of choroidal blood flow

5.6.4 Thermal simulations in the presence of choroidal blood flow

5.6.4.1 Initial temperature distribution

In Section 5.6.3.1, the initial steady state temperature distribution in the absence of choroidal blood flow was computed as the starting point for simulations predicting thermal elevation. Similarly, a new initial distribution is computed in the presence of choroidal blood flow. Once again, this is obtained by assuming a fixed choroidal blood temperature, $T_b = 37^{\circ}$ C. As before, the heating distribution in the head/eye model of Figure 5.20 is simulated, beginning at an initial assumed environmental ambient temperature of 24°C, while devoid of the influence of SAR and of power dissipation in the stimulator IC. This provides the reference point for predicting thermal elevation **above** the natural temperature distribution.

The results of this simulation are presented in Figure 5.40, with a heating distribution similar to that of Figure 5.26 where choroidal blood flow was absent. However, the new initial temperature distribution clearly highlights choroidal blood flow which is now taken into account in the thermal simulations. This can be seen in the region posterior to the retina in both eyes as compared with the same areas in Figure 5.26 where choroidal blood flow was not included.



Figure 5.40: Computed initial temperature distribution in the human head/eye model in the presence of choroidal blood flow and with no excitation from SAR or from power dissipation in the stimulator IC

The anterior portion of the initial temperature distribution corresponding to the truncated head/eye model of Figure 5.21 is again isolated from Figure 5.40 as shown in Figure 5.41. This is used to initialize the thermal simulations of SAR and of the implant IC which account for the presence of blood flow in the choroid. A peak temperature of 37.2159°C occurs in anterior portion of the initial temperature distribution, slightly higher than in Figure 5.27 due to forced choroidal blood temperature of $T_b = 37^{\circ}$ C.



Initial temperature distribution in the human head/eye model

Figure 5.41: Computed initial temperature distribution (anterior portion) in the human head/eye model in the presence of choroidal blood flow and with no excitation from SAR or from power dissipation in the stimulator IC

5.6.4.2 Temperature increase due to SAR

Under the assumption of fixed choroidal temperature, a thermal simulation predicting the temperature increase arising from the SAR of Figure 5.25 is again run with a simulated time coverage of one hour. After one hour of simulated time, the peak
Table 5.9: Temperature elevations resulting from the thermal simulation of SAR, corresponding to Figure 5.25, in the presence of choroidal blood flow

Model region ¹	Maximum	Maximum	Peak increase	Elapsed
	SAR	temperature	above initial	time
			$temperature^3$	
		Т	$\Delta T = T - T_0$	t
	$\left[\frac{\mathrm{mW}}{\mathrm{m}^3}\right]$	$[^{\circ}C]$	$[^{\circ}C]$	[minutes]
over left eye	111.9966	37.1342^2	0.0040	60
over right eye	404.1180	37.1132^2	0.0479	60

¹Corresponding to the head/eye model of Figure 5.21

²Corresponds to the forced choroidal blood temperature of $T_{blood} = 37^{\circ}C$. This happens to exceed the highest predicted steady state temperature $T_{max} = 36.7516^{\circ}C$ from the initial distribution of Figure 5.27, where choroidal blood temperature was allow not held at $37^{\circ}C$.

³These results represent the predicted steady state temperature increase in the left and right eyes between the initial and final temperature distributions

temperature rise in the right eye has converged to a value of 0.0479°C. The thermal results are summarized in Table 5.9 for each eye from the model of Figure 5.21. The peak increases encountered within each eye are proportionately lower relative to those in Table 5.7 owing to the choroid's "heatsink" effect.

A plot of temperature increase over time due to SAR for the left and right eyes is provided in Figure 5.42. In contrast to the curves of Figure 5.28, the temperature increases for both eyes appear to reach steady state around 35-40 minutes. The reason for this rapid convergence is that the fixed choroidal temperature of 37°C in the eyes prevents heat from spreading across the choroid as can be clearly seen in the color-mapped graphical plot of the steady state temperature distribution resulting from the SAR of Figure 5.25 as provided in Figure 5.43. This is in strong contrast to the situation present in Figure 5.29 where the diffusion of heat across the choroid does occur where its temperature is not forced at 37°C. The predicted steady state temperature increase of 0.0479°C is indicated by the red area concentrated in the aqueous humor of the anterior chamber forward of the lens. The fact that the isotherms over the right eye of Figure 5.43 do not cross over the choroid as they do in Figure 5.29, further indicates that the choroid is acting to provide thermal regulation. This is no longer evident near the vitreous base and over the cornea where the SAR-induced heat expands beyond the boundaries of the right eye.



Figure 5.42: Computed ocular heating versus time due to SAR in the presence of choroidal blood flow

5.6.4.3 Sensitivity to implant thermal conductivity

The study of the influence of the implant's thermal conductivity on computed temperature as described in Section 5.6.3.3 is repeated here for the head/eye model in which the choroidal blood flow condition is imposed. Once again nine thermal simulations are run on the head/eye model with choroidal blood flow present for thermal conductivity, $K_{chip} \in \{10, 20, 30, ..., 80, 90\}$ $\left[\frac{J}{m \ s \ \circ C}\right]$. A plot of the predicted steady state temperature increase over time for each value of K_{chip} is given in Figure 5.44.



Figure 5.43: Computed steady state ocular heating distribution due to SAR in the presence of choroidal blood flow

Due to the regulatory influence of blood in the choroid, the temperature increases saturate at around 30 minutes. The steady state values are plotted versus K_{chip} as shown in Figure 5.45. For each value of K_{chip} , the results indicate a lower steady-state thermal evelvation in the context of blood flow compared to the case where it is not modeled, as shown in Figure 5.31.

Once again, *xtrain* software is used to train the artificial network work of Figure 5.34 to learn the the alternative relationship between temperature increase and implant thermal conductivity in the presence of choroidal blood flow. The same network structure is employed to derive a mapping. However, the corresponding weight set will be unique to the new training data. The learned mapping is indicated by the red curve in Figure 5.45, with the network's weights and neural biases given in Equations 5.88–5.89.

Again, these apply to the neural output equations annotated on Figure 5.34. For



Figure 5.44: Computed ocular heating versus time for several values of thermal conductivity, K_{chip} , of the stimulator IC. These thermal evelations are simulated in the presence of choroidal blood flow and for expected worst case power dissipation, $P_{chip(3D)} = 46.4672$ mW.

 $K_{chip} = K_{SI} = 150 \left[\frac{J}{m \ s \ \circ C}\right]$, the network estimates a predicted steady state temperature increase of 0.4349°C, associated with the expected worst case power dissipation of $P_{chip(3D)} = 46.4672$ mW in the stimulator IC in the presence of choroidal blood flow.

$$\begin{bmatrix} w_1 \\ w_2 \\ w_3 \\ w_4 \\ w_5 \\ w_6 \\ w_7 \\ w_8 \end{bmatrix} = \begin{bmatrix} 0.0690643425275377 \\ -0.2042903912468505 \\ 0.0374010596698967 \\ 0.0289262517585018 \\ -1.9880719551736925 \\ 3.4607322734567205 \\ -1.2376819826373524 \\ -0.2964378990387502 \end{bmatrix}$$
(5.88)



Figure 5.45: Computed ocular heating versus thermal conductivity, K_{chip} , of the stimulator IC in the presence of choroidal blood flow and for expected worst case power dissipation, $P_{chip(3D)} = 46.4672$ mW.

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \\ b_5 \end{bmatrix} = \begin{bmatrix} -1.1097064676576318 \\ 1.0368998196058692 \\ -2.6216724849435793 \\ 0.0118886012385363 \\ 0.3681934957411068 \end{bmatrix}$$
(5.89)

5.6.4.4 Temperature increase due to power dissipation in the implantable stimulator IC

Again under the assumption of fixed choroidal temperature, thermal simulations are again run for each of the twelve operating conditions, using stimulator IC power estimates from of Table 3.2, in order to predict ocular heating in the left eye from the stimulator IC. Thermal results are summarized in Table 5.10.

Table 5.10: Temperature elevations resulting from the *Hspice* simulated power dissipation estimates, $P_{chip(3D)}$, of Table 3.2, in the presence of choroidal blood flow

		r -	-			-	
V_{dd}, V_{ss}	current	frame	pulse	Simulated	Peak increase above		Elapsed
		rate	width	chip power ¹	initial temperature ^{2,3}		time
					-		
	Δ	f - 1	W	P. (ap)			+
[TZ]			r 1	$^{1}chip(3D)$	$\Delta I = I - I$	r()	г. · , 1
$[V_{DC}]$	$[\mu A]$	[Hz]	[ms]	[mW]	[°C]		[minutes]
					$K_{SI} = 10^{-4}$	$K_{SI} = 150^{-5}$	
+5, -5	400	50	1	9.1862	1.0955	0.0860	60
+5, -5	400	50	2	15.1580	1.8076	0.1419	60
+5, -5	400	50	3	21.1874	2.5266	0.1983	60
+5, -5	400	60	1	10.4012	1.2403	0.0974	60
+5, -5	400	60	2	17.6018	2.0990	0.1648	60
+5, -5	400	60	3	24.8018	2.9576	0.2321	60
+7, -7	600	50	1	16.3216	1.9464	0.1528	60
+7, -7	600	50	2	27.8308	3.3188	0.2605	60
+7, -7	600	50	3	39.4527	4.7047	0.3693	60
+7, -7	600	60	1	18.7112	2.2313	0.1751	60
+7, -7	600	60	2	32.5892	3.8863	0.3050	60
+7, -7	600	60	3	46.4672	5.5412	0.4349	60

¹Duplicated from Table 3.2

 $^2\mathrm{Absolute}$ temperatures are omitted for brevity, as thermal increase above the initial distribution is the parameter of interest.

³These results indicate the predicted steady state temperature increase over the left eye between the initial and final temperature distributions encountered over the duration of the simulation.

⁴These thermal elevations are computed for microchip thermal conductivity, $K_{chip}=10 \left[\frac{J}{m \ s \ c}\right]$, according to the results plotted in Figure 5.46.

⁴These thermal elevations are K_{chip} extrapolated to silicon thermal conductivity, $K_{SI}=150 \left[\frac{J}{m \ s \ cC}\right]$, according to the trend depicted in Figure 5.45, based on the computed results from Figure 5.46, as shown in Figure 5.47.

A plot of temperature increase in the left eye over time for the twelve operating conditions is provided in Figure 5.46. As with the SAR-induced heat for fixed choroidal temperature, these temperature increases again appear to converge to steady state within 30 minutes. A plot of the temperature increase in the left eye versus stimulator IC power dissipation is provided in Figure 5.48 for the twelve operating conditions, where a linear relationship is again observed.

A color-mapped graphical plot of the predicted temperature distribution arising from operation of the implant IC is provided in Figure 5.50, corresponding to the expected worst case power dissipation, $P_{chip(3D)} = 46.4672$ mW, from Table 3.2. Due to fixed temperature of the choroid, a reduction in the predicted steady state temperature increase from 0.6123°C to 0.4349°C is now indicated over the region of the IC in the left eye. The temperature increase appears minimal near the surface of the retina. In contrast to Figure 5.39, where heat from the stimulator IC expands beyond eye region and into the surrounding head tissues, Figure 5.50 indicates a larger portion of the heat is localized by the choroid. Only near the anterior of the eye where the choroid ends does the heat spread beyond the left eye boundary.



Figure 5.46: Computed ocular heating versus time due to power dissipation in the stimulator IC for thermal conductivity, $K_{chip}=10 \left[\frac{J}{m \ s \ \circ C}\right]$ (reduced value) simulated in the presence of choroidal blood flow



Figure 5.47: Predicted ocular heating versus time due to power dissipation in the stimulator IC for thermal conductivity, K_{chip} , extrapolated to silicon thermal conductivity, $K_{SI}=150 \left[\frac{J}{m \ s \ \circ C}\right]$ (real value), while in the presence of choroidal blood flow



Figure 5.48: Computed ocular heating versus power dissipation in the stimulator IC for thermal conductivity, $K_{chip}=10 \left[\frac{J}{m \ s \ ^{\circ}C}\right]$ (reduced value) simulated in the presence of choroidal blood flow



Figure 5.49: Predicted ocular heating versus power dissipation in the stimulator IC for thermal conductivity, K_{chip} , extrapolated to silicon thermal conductivity, $K_{SI}=150 \left[\frac{J}{m \ s \ \circ C}\right]$ (real value), while in the presence of choroidal blood flow



(b) Rescaled colorbar for the distribution where microchip thermal conductivity, K_{chip} , is extrapolated to silicon thermal conductivity, $K_{SI}=150 \left(\frac{J}{m \ s \ \circ C}\right)$

Temperature (Celsius)

0.4349

Figure 5.50: Computed steady state ocular heating distribution due to expected worst case power dissipation, $P_{chip(3D)} = 46.4672$ mW, in the stimulator IC in the presence of choroidal blood flow

5.6.5 Comparison of thermal results with and without choroidal blood flow

The numerical simulations of Sections 5.6.3 and 5.6.4 clearly indicate the potential benefit which may be afforded to an implantable prosthesis by the blood flow of the choroid. However, the cooling influence may be more readily seen and appreciated by overlaying plots of temperature increase for corresponding cases involving the absence and presence of choroidal blood flow. These are given separately for the thermal increase due to SAR and the power dissipation in the stimulator IC.

Figure 5.51 offers a comparison of thermal increase in the absence and presence of choroidal blood flow over the left and rights eyes (blue and red regions, respectively) when irradiated electromagnetically according to the SAR distribution of Figure 5.25. The upper bounding curves of the blue and red regions correspond to the simulated thermal results of Figure 5.28 in Section 5.6.3 where choroidal blood flow is considered absent. Similarly, the lower bounding curves are taken from the results of Figure 5.42 in Section 5.6.4 where choroidal blood flow is considered present.

The color shaded regions between the upper and lower bounding curves represent the uncertainty region, wherein the actual temperature increase associated with the finite yet unknown choroidal blood flow rate is considered to occur. Note that the infinite blood flow approximation considered in the simulations of Section 5.6.4 is expected to closely model the response of the true biological system and therefore track the lower bounding curves much more closely that the upper bounding curves. Notice that the amount of cooling is more prominent in the right eye where the SAR (deposited electromagnetic power) is greater. However, the reduction in temperature elevation while considering blood flow relative to its absence is greater over the left eye, when expressed as a percent difference. In the presence of choroidal blood flow, the predicted steady state temperature in the right eye is lower by 0.0206°C for a decrease of 30.07% with respect to the case of no choroidal blood flow. Similarly, the maximum of the left eye is lower by 0.0039°C for a decrease of 49.37% when compared to the case of no choroidal blood flow. This data is summarized in Table 5.11.

Similarly, comparisons are provided for ocular heating due to power dissipation in the stimulator IC. These take into account the twelve simulated variations in parameters of the biphasic stimulus current pulses whose influence on ocular heating was simulated in Sections 5.6.3 and 5.6.4. Figure 5.52 offers a comparison of thermal increase in the absence and presence of blood flow over left eye, while the stimulator IC is programmed to produce biphasic stimulus pulses of 400μ A amplitude at 50Hz repetition rate. The blue, green, and red plots correspond to 1ms, 2ms, and 3ms pulse widths, respectively. Similar plots are given in Figures 5.53, 5.54, and 5.55, for 400μ A currents at 60Hz, 600μ A currents at 50Hz, and 600μ A currents at 60Hz, respectively.



Figure 5.51: A comparison of ocular heating over the left and right eyes due to SAR while considering the absence and presence of choroidal blood flow

Table 5.11: Comparison of temperature elevations resulting from simulation of SAR, corresponding to Figure 5.28 in the absence of choroidal blood flow and Figure 5.42 in the presence of choroidal blood flow

Model region	Peak increase above	Peak increase above	Difference	Percent difference
	initial temperature	initial temperature	between peak	with respect to the
	without choroidal	with choroidal	increases	case of no choroidal
	blood flow ¹	blood flow ²		blood flow
	$\Delta T_{\!_{\rm -blood}} = T - T_0$	$\Delta T_{\!+\rm blood} = T - T_0$	$\Delta^2 T = \Delta T_{\rm \!-blood} - $	$\left[\frac{\Delta^2 T}{\Delta T_{-blood}} \times 100\%\right]$
			ΔT_{+blood}	
	$[^{\circ}C]$	$[^{\circ}C]$	[°C]	
over left eye	0.0079	0.0040	0.0039	49.37
over right eye	0.0685	0.0479	0.0206	30.07

¹Duplicated from Table 5.7

²Duplicated from Table 5.9



Figure 5.52: A comparison of ocular heating over the left eye due to power dissipation in the stimulator IC for biphasic stimulus current pulses at 400μ A amplitude, 50Hz repetition rate, and 1ms, 2ms, and 3ms pulse widths, while considering the absence and presence of choroidal blood flow



Figure 5.53: A comparison of ocular heating over the left eye due to power dissipation in the stimulator IC for biphasic stimulus current pulses at 400μ A amplitude, 60Hz repetition rate, and 1ms, 2ms, and 3ms pulse widths, while considering the absence and presence of choroidal blood flow



Figure 5.54: A comparison of ocular heating over the left eye due to power dissipation in the stimulator IC for biphasic stimulus current pulses at 600μ A amplitude, 50Hz repetition rate, and 1ms, 2ms, and 3ms pulse widths, while considering the absence and presence of choroidal blood flow



Figure 5.55: A comparison of ocular heating over the left eye due to power dissipation in the stimulator IC for biphasic stimulus current pulses at 600μ A amplitude, 60Hz repetition rate, and 1ms, 2ms, and 3ms pulse widths, while considering the absence and presence of choroidal blood flow

The upper bounding curves of the color-shaded regions correspond to the simulated thermal results of Figure 5.36 in Section 5.6.3 where choroidal blood flow is considered absent. Similarly, the lower bounding curves are taken from the results of Figure 5.47 in Section 5.6.4 where choroidal blood flow is considered present. In the worst operating conditions considered, corresponding to biphasic stimulus current pulses of 600μ A amplitude at 60Hz repetition rate and 3ms pulse width, the predicted steady state temperature increase over the left eye while accounting for blood flow in the choroid is lower by 0.1774°C for a decrease of 28.97% with respect to highest temperature increase predicted with no choroidal blood flow. This comparison for the worst case power dissipation and the remaining operation conditions considered is summarized in Table 5.12.

Table 5.12: Comparison of temperature elevations resulting from the *Hspice* simulated power dissipation estimates, $P_{chip(3D)}$, of Table 3.2, corresponding to Figure 5.36 in the absence of choroidal blood flow and Figure 5.47 in the presence of choroidal blood flow

V_{dd}, V_{ss}	current	frame	pulse	Peak increase	Peak increase	Difference	Percent difference
		rate	width	above initial	above initial	between peak	with respect to
				temperature	temperature	increases	the case of no
				without	with		choroidal blood
				choroidal	chroidal		flow
				blood flow ¹	blood flow ²		
	А	$f=\tfrac{1}{T}$	W	$\Delta T_{-blood} =$	$\Delta T_{\rm + blood} =$	$\Delta^2 T = \Delta T_{\!_{\rm -blood}} -$	$\left[\frac{\Delta^2 T}{\Delta T_{-blood}} \times 100\%\right]$
				$T - T_0$	$T - T_0$	ΔT_{+blood}	
$[V_{DC}]$	$[\mu A]$	[Hz]	[ms]	$[^{\circ}C]$	$[^{\circ}C]$	[°C]	
+5, -5	400	50	1	0.1210	0.0860	0.0350	28.93
+5, -5	400	50	2	0.1997	0.1419	0.0578	28.94
+5, -5	400	50	3	0.2792	0.1983	0.0809	28.98
+5, -5	400	60	1	0.1371	0.0974	0.0397	28.96
+5, -5	400	60	2	0.2319	0.1648	0.0671	28.93
+5, -5	400	60	3	0.3268	0.2321	0.0947	28.98
+7, -7	600	50	1	0.2151	0.1528	0.0623	28.96
+7, -7	600	50	2	0.3667	0.2605	0.1062	28.96
+7, -7	600	50	3	0.5198	0.3693	0.1505	28.95
+7, -7	600	60	1	0.2465	0.1751	0.0714	28.97
+7, -7	600	60	2	0.4294	0.3050	0.1244	28.97
+7, -7	600	60	3	0.6123	0.4349	0.1774	28.97

¹Duplicated from Table 5.8

¹Duplicated from Table 5.10

A further comparison of the thermal simulation results with and without choroidal

blood flow is provided in Figure 5.56. In this figure, the predicted steady state temperature elevations occurring in the left eye is plotted against the thermal conductivity, K_{chip} , of the stimulator IC and overlayed for the two choroidal blood flow assumptions. The blue upper bounding curve is taken from Figure 5.31 of Section 5.6.3, representing thermal results in the absence of choroidal blood flow. The red lower bounding curve is taken from Figure 5.45 of Section 5.6.4, representing thermal results in the presence of choroidal blood flow.



Figure 5.56: A comparison of computed ocular heating versus thermal conductivity, K_{chip} , of the stimulator IC for expected worst case power dissipation, $P_{chip(3D)} = 46.4672$ mW, while considering the absence and presence of choroidal blood flow. This heating occurs at the location of the stimulator IC.

The grey-shaded area represents the uncertainty region between these two extremes for modeling choroidal blood flow. Both blood flow assumptions exhibit exponentially decaying trends with an asymptotically decreasing difference between the temperature elevations, for the expected worst case power dissipation, $P_{chip(3D)}$ = 46.4672mW, for which these curves apply. At the realistic value of $K_{chip} = K_{SI} = 150$ $\left[\frac{J}{m \ s \ \circ C}\right]$, a difference in temperature elevation of 0.1774°C is projected.

A final comparison of the thermal simulation results with and without choroidal blood flow is provided in Figure 5.57 in overlayed plots of temperature increase in the left eye versus stimulator IC power for the twelve operating conditions considered. As in Figure 5.56, the blue upper bounding curve is taken from Figure 5.38 of Section 5.6.3, representing thermal results in the absence of choroidal blood flow. The red lower bounding curve is taken from Figure 5.49 of Section 5.6.4, representing thermal results in the presence of choroidal blood flow.



Figure 5.57: A comparison of ocular heating over the left eye versus power dissipation in the stimulator IC for thermal conductivity, K_{chip} , extrapolated to $K_{SI}=150 \left[\frac{J}{m \ s \ \circ C}\right]$, while considering the absence and presence of choroidal blood flow

Once again, the grey-shaded area represents the uncertainty region bounding the

two choroidal blood flow assumptions. The predicted steady state temperature increase for the left eye tracks linearly with stimulator IC power dissipation both in the presence and absence of choroidal blood flow. Notice that as the power dissipation increases the difference between predicted steady state temperature elevations for the presence and absence of blood flow also increases for corresponding stimulator IC operating conditions (*ie*- for equal stimulator IC power dissipation).

5.7 Experimental validation

In supplement of the analytical validations of the numerical methods presented in Section 5.3 [143], a further step has been taken to gain additional confidence in the thermal simulation results presented in Section 5.6.3 and Section 5.6.4. Researchers at the University of Southern California (formerly at Johns Hopkins University) have experimentally measured the thermal response to power dissipation introduced into the eyes of dogs [123]. In one of several experiments in this work, 500mW of power dissipation introduced intraocularly for a duration of two hours at midvitreous using a ceramic-tipped resistive heating element led to a 2°C increase in the temperature measured at the retina surface. The simulated thermal elevations encountered in the left eye for the twelve operating conditions considered for the stimulator IC as shown in Figure 5.57, (extrapolated to thermal conductivity, $K_{chip} = K_{SI} = 150 \left[\frac{J}{m \, s \, ^{\circ}C}\right]$) represent the predicted steady state temperature increase occurring at the location of the stimulator IC model in head/eye model of Figure 5.21. In order to correlate this data with this experimental measurement at USC/JHU [123], the predicted steady state temperature increase encountered at the retinal surface is plotted versus the power dissipation in the stimulator IC as shown in Figure 5.58.

The blue upper line corresponds to the heating at the retinal surface in the absence of any choroidal blood flow. Conversely, the red lower line is associated with retinal heating where "infinite" choroidal blood flow is assumed. In the latter case, the fixed choroidal temperature of 37°C prevents the adjacent retina from heating as greatly as in the former case where the choroidal temperature is not held fixed. As such, a predicted steady state temperature increase of only 0.0038°C is computed.

Based on the observed linear dependence of retinal heating over the range of power dissipation shown here, extrapolating the 500mW power dissipation used in the experiments at USC/JHU back down to $P_{chip(3D)} = 46.4672$ mW (the highest power dissipation considered for the stimulator IC) would predict a thermal elevation of 0.1859°C. From the simulation results associated with the absence of choroidal blood flow, plotted in Figure 5.58, the thermal elevation encountered at the retinal surface for $P_{chip(3D)} = 46.4672$ mW is 0.1876°C. This is in good agreement with the measured value from the Johns Hopkins experiment [123]. Although, the data from the John Hopkins experiment was measured on live eyes with choroidal blood flow, no significant changes were measured when choroidal blood flow was stopped partway through one of the experiments [123]. The lack of any observed variations in recorded temperatures during collection of experimental data indicates that the simulation model with no choroidal blood flow. This implies that the blood vessels in the choroid are not such to maintain the choroidal temperature at a constant value of 37°C.



Figure 5.58: A comparison of ocular heating over the left eye versus power dissipation in the stimulator IC for thermal conductivity, K_{chip} , extrapolated to $K_{SI}=150$ $\left[\frac{J}{m \ s \ \circ C}\right]$, while considering the absence and presence of choroidal blood flow. This heating occurs at the inner retinal surface near the forea.

5.8 Summary

A numerical study of the thermal increase in the human eye and head associated with the operation of the implantable retinal prosthesis has been presented. A brief introduction to Maxwell's equations for characterizing electromagnetic behavior and the bio-heat equation for modeling thermal processes has been presented with a followup review of the mathematical development of numerical methods to implement these. The space-time discretization of Maxwell's equations with attention to boundary conditions has led to the *Finite Difference Time Method* (FDTD) with the integrated Perfectly Matched Layer (PML) technique, for simulating specific absorption rate (SAR) in truncated biological tissue models exposed to electromagnetic fields. This is used to numerically estimate the power deposition in a human/eye model resulting from the inductive link providing power to the *Retina-3.5* implantable stimulator IC in the retinal prosthesis. The bio-heat equation was expanded to account for additional heating sources from the SAR and from the stimulator IC. The expanded bio-heat equation was also discretized in space and time to yield a numerical method for computer implementation. Analytical validations are reviewed and applied to verify the correctness of the FDTD and thermal numerical methods.

A two dimensional human head model discretized to 0.25mm resolution was developed from imagery of an axially sliced male cadaver courtesy of the NIH *Visible Man Project.* A 0.25mm eye model was also developed from diagrammed anatomy using a custom, novel, semi-automatic discretizer to account for greater anatomical detail and was subsequently merged with the head model. The merged model was then truncated to the anterior portion including both eyes in order to lower simulation memory requirements and improve simulation time. Dielectric and thermal properties and mass densities for the constituent tissue types have been collected from the research literature. The exterior transmitter coil with 2-inch diameter and 10-turns is modeled as two opposing points sources in the two dimensional head/eye model space. The numerical FDTD method is specified to excite the equivalent magnetic field for 2A coil current in 10-turns. The resulting $\vec{\mathbf{E}}$ -field distribution yields a maximum SAR of 404 $\left[\frac{mw}{kg}\right]$ over the right eye for a $\vec{\mathbf{H}}$ -field excitation sourced from approximately one inch over the left eye.

It has been concluded that in absence of choroidal blood flow, which corresponds to the case of choroidal blood flow rates that are not sufficient to carry away a significant amount of heat, a predicted steady state temperature increase of 0.0685°C is induced by the external telemetry coil in the eye that does not contain the implanted microchip. Conversely, when considering choroidal blood flow, corresponding to the case of choroidal blood flow rates that are such to maintain the temperature of the choroid at a steady 37°C, a reduced maximum rise induced by SARs of 0.0479°C occurs.

As a results of these two dimensional simulations, the highest predicted steady state temperature increase associated with the operation of the retinal prosthesis has been shown to be due to the power dissipated by the stimulator IC, which has been evaluated under different operational conditions, corresponding to various degrees of damage of the patient's retina, and different choroidal blood flow assumptions. The highest temperature rise of 0.6123°C in the eye with the implant in the absence of blood flow and a reduced peak increase of 0.4349°C when accounting for blood flow has been recorded when computing in two dimensional simulations the temperature increase associated with the implantable microchip. It should be noted, however, that predicted steady state temperature increase induced on the retina, the most delicate organ in the human eye, was lower than 0.2°C when the implantable microchip was collocated in the center of the eyeball.

Computed results closely parallel recent experimental results in animals, especially for the case of the absence of choroidal blood flow. This suggests that actual choroidal blood flow rates are not such to enforce a constant 37°C on the choroid, as in the case of "infinite" blood flow. Further, results indicate that the proposed methods can be reliably used to guide the design of the retinal prosthesis system as it evolves from the present configuration. However, it should be noted that the proposed two dimensional methods and models are capable of capturing the temperature increase in the midvitreous above the implanted microchip, which can be lower than the actual maximum temperature on the surface of the microchip itself. Actual microchip temperatures inside the stimulator IC could be higher than predicted by the two dimensional modeling in lieu of the complex ocular geometry and the finite non-zero thickness of the microchip. The results presented for the two dimensional modeling and simulations provide a guideline for retinal and mid-vitreous heating. Three dimensional modeling is currently under consideration to provide a more accurate characterization of the temperature increase in the eye, including temperatures on the surface of the implantable chip.

Chapter 6

Future Research and Conclusion

The progress reported herein on the development of an epi-retinal prosthesis prototye system in no way represents closure of the research. Several opportunities exist for continued work on the prosthesis components. In addition, further steps can be taken in modeling the thermal response of the eye and surrounding head tissues to power dissipation in the implanted stimulator IC and to electromagnetic exposure to the extraocular radiating transmitter coil. Below is summarized some outstanding points of interest.

6.1 Future Research

6.1.1 Further work on the prosthesis hardware

1. Video integration

At present, the remote control of the stimulator IC is conducted in a manual fashion using a graphical editor, which provides access to parameters affecting stimulation waveforms generated from the implant IC. Synthetic still imagery can be synthesized by the implant by appropriately programming each stimulation circuit to elicit a phosphene within the visually field consistent with the corresponding pixel(s) from a source image. Ultimately, a practical prosthesis would derive stimulus waveforms from live video camera data. An automated interface between this camera and the prosthesis is not yet fully implemented.

2. Image processing algorithms

Since the spatial resolution available from video cameras will outpace resolution in the implants for some time, a wealth of acquired image data is available for deriving stimulator waveforms. More advanced algorithms might be implemented rather than basing stimulus waveforms from single pixel sampling of the source imagery. In addition to incorporating the additional video data, such algorithms might potentially take into account the transfer function of the human visual pathway so as to minimize the difference between the images acquired and the images perceived. The current prosthesis hardware provides a platform to begin the implementation of such algorithms.

3. Increasing spatial resolution of stimulation

Since the die area of the implant IC is a hard constraint in the prosthesis specifications, the spatial resolution is limited by the chip area required to implement each stimulus circuit. Although the current resolution of 8×8 afforded by the *Retina-3.55* IC would be a wonderful improvement over complete blindness, it is expected to be insufficient for the recovery of practical vision. Therefore, the prosthesis would benefit well from innovations such as the *multi-bias* DAC which might increase simulation resolution.

4. Extending stimulation beyond the fovea

Another improvement to impact the practical use of the prosthesis involves the area of coverage of the retina during stimulation. The delicate nature of the retina and surgical accessibility currently limits the available area on the retina to about $5\times5mm$ near the fovea. However, wide-angle human peripheral vision is accounted for as the retina occupies roughly half of the interior eyeball surface area, with generally decreasing ganglion cell densities as one approaches the outer edges. This expansive retinal area potentially offers the possibility of improving the quality of the recovered vision if the implant and the electrode array can eventually mature so as to stimulate a larger area of this retinal surface. In pursuit of this goal, developmental work is underway to realize flexible electrode arrays which can adapt to the retinal curvature [48], [49].

6.1.2 Further work on modeling and simulations

1. Threedimensional head model

The simulations presented here for estimating the thermal response of the eye and surrounding head tissues to the retinal prosthesis were conducted using two dimensional models of the head and eye. These were derived from photographed human head slices and known ocular anatomy. Of course, since heat flow is a omni-directional process, a three-dimensional model of the human head at 0.25mm resolution would be expected to produce more accurate thermal predictions than with the existing two dimensional model. Although tedious to derive, available photography from the *Visible Man* project could be used to develop such a three-dimensional model to support further thermal study.

2. Threedimensional eye model

It was the case in deriving the two dimensional head model from the *Visible Man* slice set, that the photographed eye did not provide enough clarity to derive a detailed model consistent with known ocular anatomy. Therefore, the model was derived from "to-scale" sketches of human eye cross-sections. A similar process would need to take place for deriving a threedimensional model. Fortunately, the human eye is symmetrical about an axis passing through the iris and lens, excluding the off-center optic nerve and the muscles attaching the sclera. This

fact can be used to "rotate" two dimensional sketches about this axis to provide a three-dimensional source for sampling a 0.25mm three-dimensional model to be subsequently "embedded" in a three-dimensional head model of the same resolution.

3. Parallelization of FDTD the algorithm

The storage requirements of a threedimensional head/eye model discretized to 0.25mm resolution would stress the memory capabilities of modern single CPU PCs, even those with gigabytes of RAM. Furthermore, the speeds of current single CPU machines are insufficient to simulate such a threedimensional head model in a reasonable amount of time. This problem could be addressed with either a networked collection of single CPU machines or else a multi-processor machine (*ie*-supercomputer). Accordingly, the FDTD implementations of the electromagnetic and thermal algorithms could be recoded such that the model can be divided and piece-wise assigned to multiple processors with communication provisions made at the regional boundaries where information must be shared between processors.

4. Removal of the lens and inclusion of the secondary coil

Obviously, in a prosthesis for the blind, the optical properties of the crystalline lens are not necessary. In fact, the lens cavity can provide a surgically accessible location for anchoring prosthesis components, including the implanted power and data recovery (secondary) coil. Once coil geometry and orientation are finalized, the eye model can incorporate the presence and structure of the coil in the lens cavity.

5. Accounting for power recovery circuits

Power dissipation from implanted components was considered only for the microstimulator IC (*Retina-3.55*), which does not include power recovery circuits such as the power carrier rectifier and regulator. These will account for additional power dissipation and are expected to yield higher predictions of ocular heatings from the numerical thermal FDTD. Once these circuits are designed and included in the prosthesis, the head and eye models can be expanded to incorporate models of these components.

6. Inclusion of power dissipated in the retina

Since the retina has a measurable impedance, a fraction of the total power consumption of the implanted components is accounted as dissipation in the retinal tissue. This can also be included in further simulations to predict ocular heating, especially in the vicinity of the area of retinal stimulation.

6.2 Conclusion

A backpack unit is presented as a portable stimulation unit for evaluating retinalprostheses in animals. The unit can be interfaced to a host PC for configuration, control, and monitoring. Once configured with stimulation instructions, the unit is autonomous and can be detached. Hardware support for image acquisition and processing is included in the backpack for future connection to an external camera. A PGA-packaged sixty-channel micro-stimulator, *Retina-3.5*, is included in the backpack for extra-ocular electrical stimulation of retina through a twenty-five site silicone-platinum electrode array. Complete control of the stimulator can be maintained from the host PC. In future experiments, where the micro-stimulator is implanted, the backpack can again be used to control the stimulator through a wireless telemetry link. The literature review on biotelemetry has summarized the current efforts and progress toward wireless telemetry links for bio-implants. The efficient design of these links is deceptively simple when considering the low emphasis to which the link is delegated in the system-level perspective of a prosthesis design. Typically, the neuro-stimulator or neuro-recorder receives greater emphasis in the prosthesis design effort. The literature reveals that significant engineering effort is needed to realize an efficient link. Infrared links are usually limited to applications where optically conducive, such as in the retinal prostheses. Therefore, the inductive link based on coils continues to be the most popular form for wireless power and data delivery. Amplitude shift keying and on-off shift keying (OOSK) of the power carrier appear as the dominant modulation schemes for data delivery because of the resonant condition of coil-based telemetry links, although angle modulation schemes (FSK/PSK) are well known to be more error-robust. Back-telemetry schemes published in the literature appear presently to be implemented using either integrated active transmitters or with passive schemes, such as load impedance modulation and reflection.

An implantable micro-stimulator has been presented for use in the epi-retinal prosthesis system. The stimulator is designed and implemented in AMI-1.2 μ m CMOS. It is programmable in real-time from external prosthesis hardware with configuration data and run-time image data at frame rates up to several hundred images/sec. Sixty unmultiplexed stimulus driver circuits can be programmed with independent pulse amplitudes to represent images intensities consistent with acquired data such as from an external mini-camera. Global shared pulse timing parameters are programmable from the host. Error detection mechanisms are implemented on-chip to prevent the generation unintended stimulation currents resulting from erroneous data.

A modified binary weighted DAC structure for implantable neuro-stimulators has

been presented which occupies significantly less area that a conventional DAC structure. The architecture preserves robust layout techniques for current mirrors in order to maintain linearity, accuracy, and repeatability across the chip, without compromising the savings in area. Transistor counts are reduced from $2(2^N - 1)$ FETs for an 2N-bit conventional binary-weighted DAC using simple mirrors to N FETs for the reduced area DAC. Die area savings for an 8-bit DAC are approximately 52%, with possible higher savings with tighter layout afforded by newer IC processes with more metal layers. The benefits should prove beneficial for increasing spatial resolution in micro-stimulators and consequently the effectiveness of visual prostheses.

A numerical study of the thermal increase in the human eye and head associated with the operation of the implantable retinal prosthesis has been presented. A brief introduction to Maxwell's equations for characterizing electromagnetic behavior and the bio-heat equation for modeling thermal processes has been presented with a followup review of the mathematical development of numerical methods to implement these. The space-time discretization of Maxwell's equations with attention to boundary conditions has led to the *Finite Difference Time Method* (FDTD) with the integrated Perfectly Matched Layer (PML) technique, for simulating specific absorption rate (SAR) in truncated biological tissue models exposed to electromagnetic fields. This is used to numerically estimate the power deposition in a human/eye model resulting from the inductive link providing power to the *Retina-3.5* implantable stimulator IC in the retinal prosthesis. The bio-heat equation was expanded to account for additional heating sources from the SAR and from the stimulator IC. The expanded bio-heat equation was also discretized in space and time to yield a numerical method for computer implementation. Analytical validations are reviewed and applied to verify the correctness of the FDTD and thermal numerical methods.

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As a results of these two dimensional simulations, the highest predicted steady state temperature increase associated with the operation of the retinal prosthesis has been shown to be due to the power dissipated by the stimulator IC, which has been evaluated under different operational conditions, corresponding to various degrees of damage of the patient's retina, and different choroidal blood flow assumptions. The highest temperature rise of 0.6123°C in the eye with the implant in the absence of blood flow and a reduced peak increase of 0.4349°C when accounting for blood flow has been recorded when computing in two dimensional simulations the temperature increase associated with the implantable microchip. It should be noted, however, that predicted steady state temperature increase induced on the retina, the most delicate organ in the human eye, was lower than 0.2°C when the implantable microchip was collocated in the center of the eyeball.

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