An Arbitrary Waveform Stimulus Circuit for Visual Prostheses using a Low Area Multibias DAC

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Abstract

Retinitis pigmentosa and age-related macular degeneration lead to blindness through progressive loss of retinal photoreceptors. Attempts are underway to construct a visual prosthesis to recover a limited sense of vision for these patients with the aid of implantable electronic devices. The function of these microchips is to provide electrical stimulation to existing viable retinal tissues, using an array of on-chip stimulus circuits. This paper describes a key improvement to our existing retinal stimulator designs which is a new stimulus circuit with significantly decreased implementation area and the ability to support arbitrary stimulus waveforms, given that an array of such stimulus circuits is required, thereby yielding more stimulus circuits per unit chip area and thus greater spatial resolution in stimulation. We also introduce DAC gain prescalar and DC-offset circuits which tune the stimulus circuits to the optimal effective range for each patient due to variation in retinal degradation. The prototype chip was fabricated by MOSIS in 1.2μm CMOS technology.

Index Terms

Retinitis-Pigmentosa, Age-Related Macular Degeneration, Retinal-Prosthesis, Visual-Prosthesis, Electrical Stimulation, DAC

I. INTRODUCTION

Age Related Macular Degeneration (AMD) and Retinitis Pigmentosa (RP), among the leading causes of blindness [1], effect over 10 million people worldwide through progressive photoreceptor

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loss (rod/cones) in the retina [2]. Attempts are underway to construct visual prosthesis to recover a limited sense of vision for these patients using implantable electronic devices to electrically stimulate existing viable retinal tissues using an array of on-chip stimulus circuits. The demonstration that direct electrical stimulation of retinal ganglion cells can create visual sensation in patients has been shown clinically [3]. Controlled biphasic charge-balanced current signals in this range delivered to degenerate retina can elicit the perception of phosphenes, or spots of light, in blind patients. By stimulating several adjacent locations simultaneously on the retina patients can experience multiple phosphenes which convey an image when viewed collectively. Patients have been able to recognize alphabetic characters and other simple patterns when stimulated by a small array (eg- 3×3 or 5×5) of retinal electrodes. This opens the possibility of an electronic prosthesis to bypasses the defective photoreceptors. Several studies have investigated the effectiveness of low-resolution vision [3], [4]. Results from [5] indicate that larger electrode size/spacing increases the difficulty in detecting facial features. Images of only two gray levels are insufficient for resolving facial detail. A reduction in electrode count from 25×25 to 16×16 requires more manual "scanning" across the scene to offset "tunnel vision". This was exacerbated when increasing the pixel dropout percentage. Based on these insights, innovative circuit topologies yielding greater spatial or intensity resolution through reduced circuit area would be valuable to visual prostheses. Furthermore, differing degrees of retinal degeneration among patients requires various forms of stimulation patterns.

Numerous stimulators designed for visual prostheses [6]–[8] use current-mode DACs which switch currents weighted in powers of two. Although, this does provide linearity as good as with "thermometer-coded" DACs [9] and requires the same amount of analog circuitry [10], the binary weighted DAC requires no decoding of the digital input, justifying its popularity in implantable devices where area is a premium. The major disadvantage of both DACs for implantable stimulators is an implementation area which grows exponentially with resolution.

In [11], a DAC implementation is reported with circuit area reduced to 0.01mm^2 in 1.2μm for 5-bit resolution in which device widths and lengths are varied together to achieve a powers of two current weighting. Since tracking performance between in current mirrors can suffer from V_t variation, process variation in device geometry, or from channel length modulation [12], this approach may lead to non-monotonicity in the DAC transfer function. The *multi-bias* DAC offers an alternative where devices of fixed width and length are used in a low area topology while retaining low INL and DNL. The circuit area scales linearly versus number of bits instead of exponentially, yielding more stimulus circuits per chip area and thus greater stimulus resolution.

The paper is organized into five sections. Section II introduces the novel *multi-bias* concept and how this leads to a lower implementation area over conventional stimulus circuits. Section III discusses circuit implementation. Section IV provides experimental measurements while Section V offers additional insights from circuit simulation. Section VI covers improvements and design enhancements in future revisions with concluding remarks in Section VII.

II. Proposed Improvement: *The Mutli-bias DAC*

Currents in the binary-weighted DAC derive from a shared FET gate bias which is produced in a single reference branch. This is distributed across the DAC branches to reproduce the output currents. Binary weightings of currents are controlled using device geometries and are defined as $\mathrm{i}_n = K\frac{2^n W}{L}(V_{ref} - V_t)^2$, for $0 \leq n \leq N$ (neglecting channel length modulation). For an N-bit DAC of simple current mirrors, this requires $2^N - 1$ transistors of size $\frac{W}{L}$. The modification developed for the *multi-bias* DAC is to replace the single fet-gate bias, V_{ref}, with multiple gate biases, $(V_{bias_N-1}, V_{bias_N-2}, \ldots, V_{bias_1}, V_{bias_0})$ with N transistors all sized at $\frac{W}{L}$ instead of $2^N - 1$ transistors. Then, the drain currents for the N-bit DAC become $\mathrm{i}_n = K\frac{W}{L}(V_{bias_n} - V_t)^2$. This new technique is referred to as the *multi-bias* DAC, because each DAC branch uses an independent FET gate bias. Hence, relative currents are controlled by gate bias rather than by geometry. This permits each branch to use identically sized devices, which is the key to area reduction while preserving device

tracking, as shown in Figure 1a for an 8-bit DAC. The biases are generated using currents drawn through diode connected FETs with the aid of a conventional binary weighted DAC, as shown in Figure 1b. Although this second DAC would appear to impart a high area penalty, it is instantiated only once per chip to service a much larger array of reduced area stimulus circuits based on *multi-bias* concept. The bias voltages, $V_{bias_{N-1}}$-V_{bias_0}, are therefore generated centrally and distributed to all of the DACs throughout the stimulator.

III. Circuit Implementation

A. Architecture

The architecture of the prototype chip for the proposed stimulus circuit is shown in Figure 2. It is programmed serially using digital *clock* and *data* input pins. The chip processes a *configuration* packet and a *stimulus* data packet. Digital data is shifted into 15-bit fifo Q_{14}-Q_0 on each *clock* cycle and is then latched into either a 15-bit *configuration* data register using the *load-config* input or else into an 11-bit *stimulus* data register using the *load-DAC* input. Bits R_5-R_0 tune the adjustable resistance in the current reference circuit (or select an off-chip R_{bias} using R_E), bits G_3-G_0 program the current gain prescalar (discussed in subsection III-D.1), bits O_5-O_0 program the *multi-bias* DC-offset DAC (discussed in section III-D.2), and bits D_7-D_0 of the stimulus data register program the 8-bit *multi-bias* stimulus DAC (discussed in subsection III-B). The current outputs from the stimulus DAC and the DC-offset DAC are summed and passed into the biphasic current output amplifier. Bits *A*,*C*, and *S* determine current steering within the output amplifier (discussed in subsection III-C), to produce either an anodic or cathodic current pulse.

B. 8-bit wide-swing cascoded multi-bias DAC

INL and DNL in the transfer characteristic of the *multi-bias* DAC are sensitive to correctly scaled currents in the DAC branches. Each branch current, i_k, associated with digital input bit, D_k, should be twice the magnitude of branch current, i_{k-1}. Therefore, we have investigated the perfor-

mance of a wide-swing cascoded form of the *multi-bias* DAC, as shown in Figure 3. This structure provides increased output impedance for improved branch current tracking, while requiring only one additional cascode bias to be distributed to the DACs.

C. Biphasic output current amplifier

The current i_{DAC} from the *multi-bias* DAC is passed into a biphasic current amplifier, which acts as an output stage to drive the tissue impedance and is detailed in Figure 4. The current from the DAC is passed into NFETs M_1 and M_2, which form the reference branch of a wide swing cascode mirror formed with M_5 and M_6 (for producing the anodic pulse) and with M_9 and M_{10} (for producing the cathodic pulse). Output stage FETs M_7, M_8, M_9, and M_{10} are 30 times wider in order to mirror the *multi-bias* DAC up to full-scale level of 400μA [13]. Logic signals A,$\overline{A}$ and C,$\overline{C}$ control complementary switches to enable or disable the anodic (M_3-M_8) and cathodic currents (M_9, M_{10}) currents, respectively. As this output stage is intended for our epi-retinal prosthesis [8], the combined electrode/retina impedance is modeled with the load resistance, R_{LOAD}. Although the value of this load varies with geometry of the electrode, extent of retinal degeneration, and frequency of stimulation, impedances on the order of 10kΩ have be observed experimentally [14]. Wide-swing cascode current mirrors are used in the output stage to achieve maximize output current per supply voltage while maintaining FET operation in the saturation region [10].

D. Gain/offset scaling of stimulus currents

Generally, more advanced retinal degradation is accompanied by a greater stimulation threshold requiring a minimum current, $i_{threshold}$, is to elicit perception. Moreover, sensitivity in perception to brightness variation should saturate at some current amplitude, $i_{saturation}$, with no change in perception from increased stimulus currents. The prototype IC implements a gain pre-scalar and a DC-offset DAC which produce a current *gain* and *offset* to define $i_{threshold}$ and $i_{saturation}$. These es-

tablish the operating range of the the 8-bit *multi-bias* DAC such that $i_{threshold} \leq i_{stimulus} \leq i_{saturation}$ from the output amplifier. This prevent the loss of stimulus resolution over the domain of excitation currents which are effective for eliciting perception. This provides greater flexibility for device optimization compared with our previous IC design [8].

D.1 Programmable current gain prescalar

The gain prescalar circuit, shown in Figure 5, allows the master reference current to be scaled from $\frac{1}{16}$th to 100% of its nominal value with 4-bit linear resolution. A copy of the reference current is reproduced from biases V_{ncasc} and V_{nsrc} in NFETs M_3 and M_4, which is passed to the wide-swing cascoded reference branch of M_1 and M_2. This current is fractionally mirrored into the binary weighted branches of M_5-M_{14}, thus implementing a 4-bit conventional wide-swing cascoded current-mode DAC. The complementary switches controlled by G_3-G_0 enable the DAC branches by switching the gate potential of the current source PFETs (M_7, M_9, M_{11}, and M_{13}) to either the bias voltage from the reference branch (ON state) or to V_{dd} (OFF state). The unswitched branch of M_5 and M_6 prevents a gain of zero such that G_3-G_0=0000 does not yield zero current. Selected current from the prescalar DAC is passed to NFETs M_{15} and M_{16} and then mirrored into the *multi-bias* generator, to supply bias potentials for the stimulus DACs. The prescalar current programmed by G_3-G_0 establishes a full-scale current over which the *multi-bias* DAC exercises its 8-bit resolution using bits D_7-D_0. The gain pre-scalar is implemented only once the chip to establish a global shared current gain for all of the *multi-bias* stimulus circuits on chip.

D.2 Programmable *multi-bias* DC-offset DAC

The offset DAC shown in Figure 6 provides the minimum current of $i_{threshold}$ by implementing a 4-bit current mode DAC which again scales the master reference current from zero to its nominal value. The DC-offset DAC is contained in each stimulus circuit and so is implemented using the proposed *multi-bias* concept to reduce area. Accordingly, it taps gate bias voltages from the

central *multi-bias* generator. The DAC is implemented with PFETs M_1-M_8 equally sized, which implement wide-swing cascoded current mirrors in the same manner as in the *multi-bias* stimulus DAC. Bits O_3-O_0 control complementary switches to enable or disable the DAC branches. The selected current is connected in parallel with the current from the 8-bit *multi-bias* stimulus DAC, summing the two current into the load (recall from Figure 4).

E. Multi-bias generator

The *multi-bias* generator, shown in Figure 7, is a centrally located circuit which produces gate bias potentials for all the *multi-bias* DACs. It is analogous to Figure 1b with the exception that the devices are now wide-swing cascoded. The bias voltages of V_{pref1}, V_{pref2}, V_{ncasc}, $V_{pcasc(Vdd)}$, and $V_{pcasc(Vcc)}$ are produced in a tunable current reference circuit based on the type from our prior stimulator IC design [8], with the addition of a digitally adjustable biasing resistance to tune the reference current. This reference current is mirrored to M_1 and M_2 and subsequently passed to M_3 andM_4. NFETs M_{21}-M_{28} and M_{29}-M_{36} form the wide-swing cascoded weighted DAC which mirrors this reference current in binary weighted fractional increments. The resulting current-source bias potentials V_{Dbias7}, V_{Dbias6},...,V_{Dbias0} along with the cascode bias $V_{pcasc}(Vcc)$ form the set of biases which are distributed to the *multi-bias* stimulus DACs.

IV. MEASURED RESULTS

The prototype chip was fabricated in 1.2μm CMOS with a die size of 2.2mm$\times$2.2mm. Measurements are taken of the circuit's output current delivered to the load resistance, R_{LOAD}=10kΩ, as shown in Figure 4. An important design criteria in circuits for bio-implantable neuro-stimulators is that biphasic currents be charge-balanced in order to protect the electrodes. Therefore, the performance of the new *multi-bias* DAC in Figure 3 and the output amplifier of Figure 4 is characterized in terms of linearity, accuracy (or tracking) and power supply sensitivity.

A. Gain pre-scalar measurement

In measuring the performance of the gain prescalar, the current reference circuit is tuned to yield $i_{stimulus}$ of 400μA. Sixteen separate measurements were taken, one for each setting of the 4-bit prescalar circuit. For each gain setting the digital input to the 8-bit *multi-bias* stimulus DAC was swept from 00(hex) to FF(hex). This produces a stimulus current, $i_{stimulus}$ in R_{load} ranging from 0 to the maximum value determined by prescalar current ($\times$30), with a full-scale expected anodic and cathodic current of 400μA. The DC-offset DAC of Figure 6 was set to O_3-O_0=0000 during these measurements. The experimental measurements overlayed and shown in Figure 8 indicate that the gain prescalar can effectively vary the full-scale $i_{saturation}$ value.

B. DC-offset measurement

In measuring the performance of the DC-offset DAC, sixteen separate measurements are again taken for each selectable offset level. For each setting the digital input to the 8-bit *multi-bias* stimulus DAC is swept from 00(hex) to FF(hex). This yields a stimulation current $i_{stimulus}$ in R_{load} ranging from a minimum value established by the DC-offset DAC ($\times$30) to a maximum value determined by the prescalar current ($\times$30), with a full-scale expected anodic and cathodic current of 400μA. At $V_{dd}/V_{ss} = \pm$5v load current much beyond 400μA will force PFETs M_7-M_{10} of the biphasic amplifier into the linear region and will clip the output current. This is evident in the curves of Figure 9, where the gain prescalar is programmed at a setting of $<G_3$:$G_0>$=1000(binary), corresponding to a full-scale load current of approximately 260μA. For this setting, a DC-offset programmed setting near $<O_3$:$O_0>$=0111(binary) and beyond will lead to clipping. In practice the gain prescalar and offset DAC would together be programmed to implement $i_{threshold}$ and $i_{saturation}$ current limits within the drive capabilities of the stimulus circuits. The experimental measurements shown in Figure 9 indicated that the *multi-bias* DC-offset DAC wired in parallel with the stimulus DAC can effectively establish $i_{theshold}$ to conserve resolution in the stimulus DAC.

C. Linearity

Linearity in the DAC's transfer characteristic is useful for characterizing the effectiveness of tissue stimulation as a function of current amplitude. Thus, we measure the INL and DNL errors in the currents delivered to R_{LOAD}. INL is measured with respect to a straight line connecting the endpoints, for which the error in the anodic and cathodic currents is shown in Figures 10a and 10b. Maximum error is -3.11 and 1.59, respectively. The DNL error in the anodic and cathodic currents is shown in Figures 10c and 10d, for which maximum errors are 2.15 and 2.11, respectively. Circuit simulations show that the *multi-bias* DAC concept is susceptible to DNL errors. We discovered that the reference currents in FETs M_5–M_{20} in the *multi-bias* generator (Figure 7) and the mirrored currents in FETs M_1–M_{16} of the *multi-bias* DAC (Figure 3), did not match precisely, but were instead mirrored to the DAC with positive offsets which became progressively larger for the higher-order bits. The source of these offsets is related to the difference in impedance between FETs M_5–M_{20} in the *multi-bias* generator and FETs M_1 and M_2 in biphasic amplifier into which the *multi-bias* DAC delivers its current, i_{DAC}. As the widths of M_5–M_{20} increase from $\frac{W}{L}(1\times)$ to $\frac{W}{L}(128\times)$ the discrepancy in mirrored current increases. When stepping through the DAC digital input in a binary fashion, these current offsets lead to negative DNL errors at each major bit transition (...00000111→00001000, 00001111→00010000,...,01111111→10000000). We were able to reduce the non-monotonicity in the wide-swing form of the *multi-bias* DAC by increasing the widths of M_6 and M_{14} to $\frac{2W}{L}$ and M_5 and M_{13} to $\frac{4W}{L}$ in the *multi-bias* generator (Figure 7) with identical changes to M_2, M_{10}, M_1, and M_9 in the *multi-bias* DAC (Figure 3).

D. Accuracy

We measure the accuracy in terms of the tracking between the anodic and cathodic currents. Figure 11 provides the current amplitude of the two currents delivered into R_{LOAD} for a full-scale $i_{stimulus}$ value of 400μA at $V_{dd}/V_{ss} = \pm 5.5$v. The measurement shows that the anodic current is

less by an amount equal to 14.56 LSB at D_7–D_0=FF_{16} or 5.74% with respect to the cathodic current. The charge-imbalance on electrodes due to this mismatch could be depleted with a charge cancellation or shorting circuit in the output stage briefly connecting R_{LOAD} to the ground return potential [8].

E. Power supply sensitivity

When a neuro-stimulator is powered inductively, relative movement between exterior and interior coils will cause a modulation of the DC supplies to the chip. To characterize the sensitivity to this, we measure the anodic and cathodic currents, $i_{stimulus}$ for $5\text{v} \leq V_{dd} \leq 7\text{v}$ and $-7\text{v} \leq V_{ss} \leq -5\text{v}$. Results in Figure 12 show good supply immunity for full-scale current amplitudes in $i_{stimulus}$ of of 200μA and 400μA, with $2.5\frac{\mu\text{A}}{\text{V}}$ measured for the 400μA anodic current.

F. Area reduction

A summary of the experimental measurements and simulations results is provided in Table I. A die photograph of the prototype chip is shown in Figure 13. The die measures 2.2mm$\times$2.2mm and was fabricated in the AMI-1.2μm CMOS process through MOSIS. The area occupied on the chip by the 8-bit *multi-bias* generator is 0.177mm^2, which while appearing significant is incurred only one per chip to service an array of *multi-bias* DACs. The binary weighted DAC employed within the *multi-bias* generator occupies an area of 0.107mm^2. The *multi-bias* DAC on the other hand consumes 0.0265mm^2, for a savings of 75% compared with the conventional binary current-weighted DAC, with potentially higher savings from tighter layout in more advanced IC processes having more metal layers for routing the bias potentials.

V. The fully-cascoded topology

Although not fabricated on the test chip, we subsequently discovered that a fully-cascoded form of the *multi-bias* generator and DAC, shown in Figure 14, is more immune to non-monotonicities

because of the higher output impedance of this circuit structure and therefore produces negligible offsets in the mirrored currents yielding improved INL and DNL. Circuit simulation yields curves similar to those in Figure 10 with lower INL errors of 1.31 and 0.45 for the anodic and cathodic currents, respectively, and reduced DNL errors of -0.55 for both currents. This improvement in INL and DNL comes at the expense of a greater number of bias potentials which must be distributed to the DACs (eight current source biases plus eight cascode biases, for a total of 16 per DAC for 8-bit resolution).

A. Sensitivity of bias voltages to noise

A sensitivity analysis of *multi-bias* DAC branch currents to bias noise is summarized in Table II. These branch currents correspond to i_7–i_0 as annotated on the fully cascoded *multi-bias* DAC of Figure 14. In this study, the branch currents were simulated with $\pm$10mv of DC noise offset from the nominal values of the eight current-source bias potentials, $V_{DbiasS7}$–$V_{DbiasS0}$ of PFETs M_5–M_{12}, and the eight cascode bias potentials, $V_{DbiasC7}$–$V_{DbiasC0}$ of PFETs M_{13}–M_{20}. As expected, the noise on biases $V_{DbiasS7}$–$V_{DbiasS0}$ imparts greater current disturbance than noise on biases $V_{DbiasC7}$–$V_{DbiasC0}$. Furthermore, the lower significant bits exhibit more sensitivity expressed in percent difference. However, in spite of a lower sensitivity to noise in the higher order bits, as the nominal currents increase by factors of two, the $\pm$10mv of bias noise results in a larger absolution deviation in the current. If routing resources allow, a better solution would provide grounded shielding for all sixteen bias potentials. If a compromise must be made, then shielding preference should be given to the current source biases, $V_{DbiasS7}$–$V_{DbiasS0}$, owing to their greater sensitivity to noise.

B. Thermal sensitivity of the Multi-bias *DAC*

Figure 15 provides insight into the temperature sensitivity of the current outputs of the 8-bit *multi-bias* DAC and the biphasic current amplifier. The temperature swings in centered at 37°C

associated with human body temperature as would be the case when the chip is implanted The curves of Figure 15 consider a coverage of $\pm 10^{\circ}$C around a nominal body temperature of 37°C. Current outputs from the multi-bias DAC exhibits a nearly linear dependence with a sensitivity of $-0.0249\frac{\mu A}{^{\circ}C}$, over the range of 27°C–47°C. The anodic current from the biphasic amplifier exhibits a slope of $0.5421\frac{\mu A}{^{\circ}C}$, over the same range, while the cathodic current yields a slope of $0.7154\frac{\mu A}{^{\circ}C}$. The greater sensitivity of the PMOS mirrors (anodic) over the NMOS mirrors (cathodic) indicates that current amplitude mismatch will gradually increase for elevated temperature. However, we do not expect to see this in practice since numerical, iterative thermal simulations based on the *bioheat* equation [15] have indicated that an increase of 0.4°C–0.6°C in implanted chip temperature with 0.2°C elevation at the retina could occur due to power dissipation in our 60 channel retinal-stimulator IC [8] implanted in an anatomically derived 2D head/eye model [16].

VI. Improvements and design enhancements

One concern of the *multi-bias* concept to reduce area regards the impact of noise on the bias voltages. Future implant ICs will contain arrays of hundreds of stimulator circuits, with the bias potentials of the *multi-bias* DACs distributed across the chip from the central *multi-bias* generator. Two foreseeable sources of noise exist. Our recent stimulator devices [8] are mixed signal designs with digital clocks and data distributed throughout the chip alongside analog DC bias potentials with capacitively coupled noise. In the AMI-1.2μm process with its two metal layers, there is limited routability to protect the bias potentials from noise on adjacent interconnect and from noise injected into the substrate. In more advanced IC processes with more metal layers, all of the *multi-bias* potentials can be collected into a common group with grounded interconnect of either side of the group and grounded metal shield planes above and below the group [17]. However, when the complementary switches in the *multi-bias* DACs toggle state, clock feedthrough noise can couple onto the *multi-bias* interconnect and affect other *multi-bias* DACs sharing those biases. Replacing these switches with single FET pass gates in series with the branch current will remove

clock feedthrough noise onto the bias voltages, albeit at the cost of higher V_{cc} necessary to keep the DAC FETs saturated. In this configuration, the unswitched bias potentials connect directly to the FET gate terminals and provide additional noise immunity in that the biases are ”buffered” by the combined gate capacitances of all the *multi-bias* DACs. Noise associated with series switching the branch current should not be problematic as it relates to electrical stimulation in our retinal prosthesis. Since the time scale of this noise is much shorter than the stimulus pulse widths needed for ganglion cell excitation [18], [3] and is shorter than the refractory times of the neurons/cells [19], it is not expected to elicit perceptual artifacts.

VII. Conclusion

We have introduced key improvements to the stimulus circuit used in our existing retinal stimulators designs. The gain prescalar and DC-offset circuits allowed the stimulus circuits to be tuned to compensate for variations in retinal degradation per patient. In additional, a novel modification to the conventional binary-weighted current-mode DAC based on distributed multiple bias potentials was presented to significantly reduce implementation area. Measured INL and DNL of -3.11 and 2.15, respectively, were obtained with even better metrics expected from the fully-cascoded topology. Anodic and cathodic current tracking within 5.74% was experimentally measured with good supply insensitivity of $2.5\frac{\mu\text{A}}{\text{V}}$ recorded. The *multi-bias* approach significantly decreases the circuit area compared with the conventional DAC structure, resulting in a linear instead of exponential increase in area versus resolution. Transistor counts are reduced from $2(2^N-1)$ FETs for an N-bit conventional binary-weighted DAC using cascoded mirrors to $2N$ FETs for the reduced-area *multi-bias* DAC. Area savings for an 8-bit DAC are approximately 75%. The benefits of reduced area will be beneficial for increasing spatial resolution in stimulator devices and consequently the effectiveness of visual prostheses.

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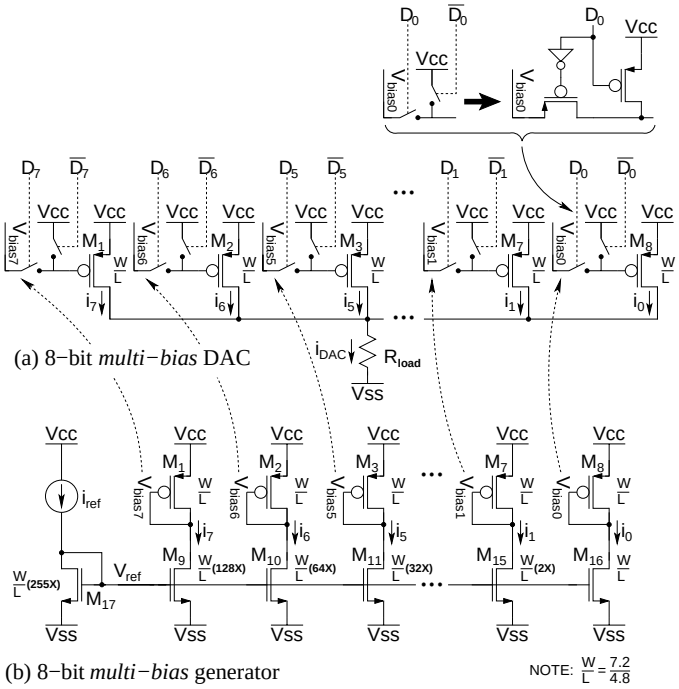


Fig. 1. *Multi-bias* DAC concept introduced with simple PMOS current mirrors

TABLE I

CHIP PERFORMANCE SPECIFICATION AND MEASUREMENTS

Technology	MOSIS 1.2μm CMOS
Die size	2.2mm $\times$ 2.2mm
Area	
multi-bias generator	0.177mm^2
multi-bias DAC	0.0264mm^2
conventional binary current-weighted DAC	0.107mm^2
biphasic amplifier	0.0237 mm^2
Amplitude resolution	8-bits
Anodic current INL	-3.11
Cathodic current INL	1.59
Anodic current DNL	2.15
Cathodic current DNL	2.11
Anodic/Cathodic mismatching	14.56 LSB (5.74%)
Supply sensitivity	2.5$\frac{\mu A}{V}$

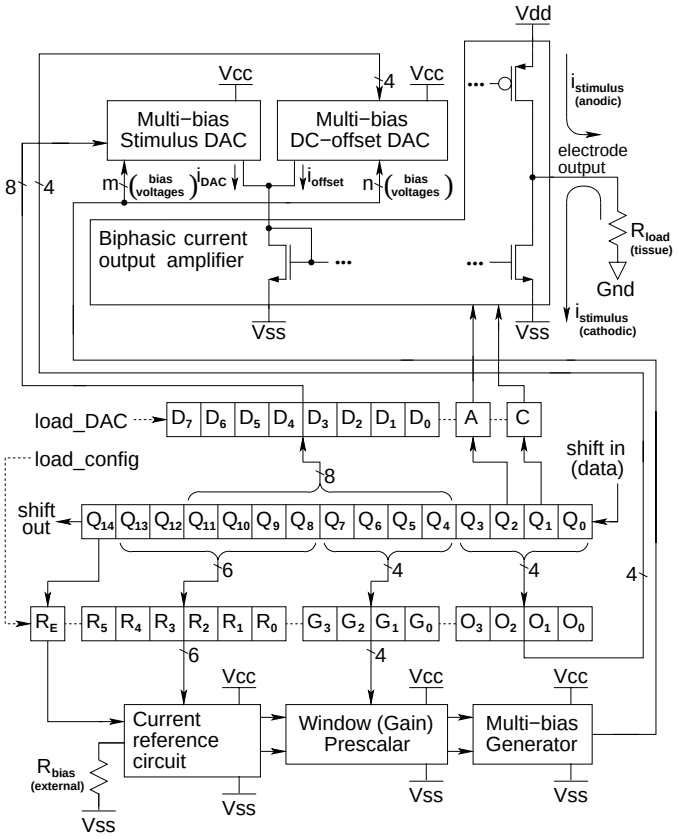


Fig. 2. System block diagram for the Reduced-area (*multi-bias*) DAC prototype chip

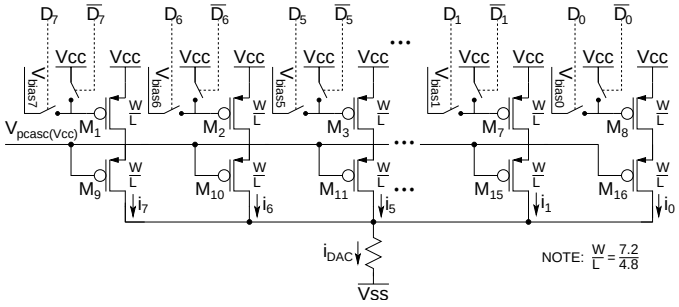


Fig. 3. Wide-swing cascoded configuration of the *multi-bias* DAC

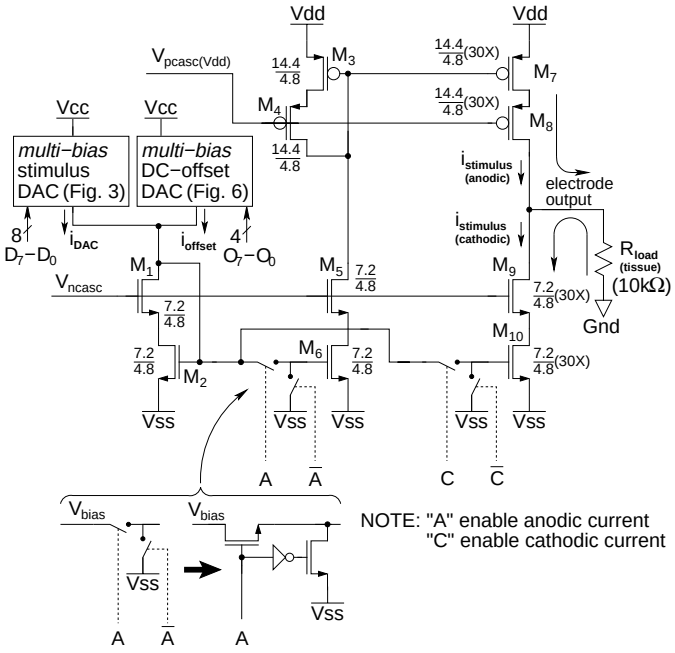


Fig. 4. Biphasic current output amplifier

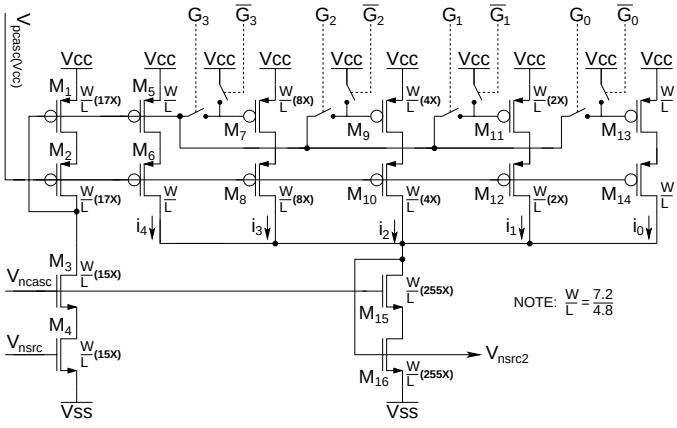


Fig. 5. Digitally programmable 4-bit reference-current gain-prescalar circuit

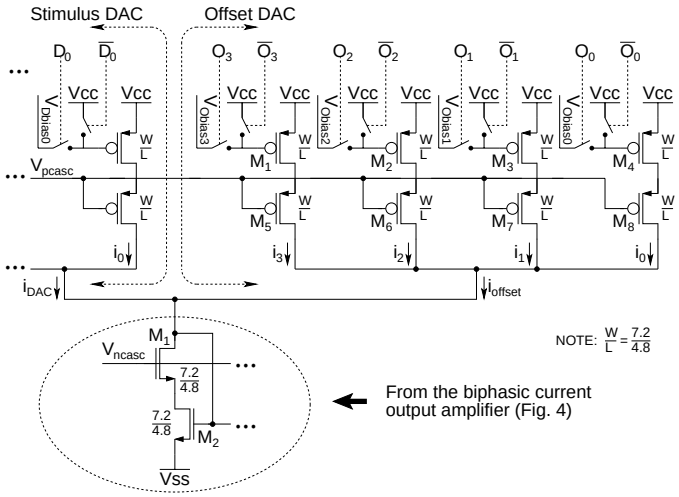


Fig. 6. Digitally programmable 4-bit *multi-bias* DC-offset DAC (in parallel with the 8-bit *multi-bias* stimulus DAC)

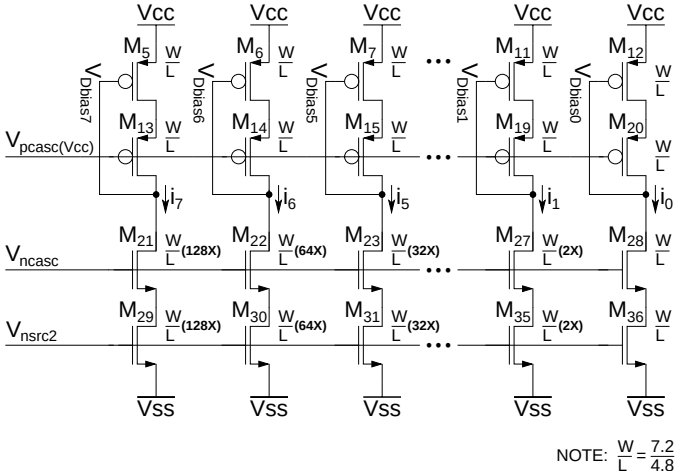


Fig. 7. Wide-swing cascoded, 8-bit *multi-bias* generator (biases shown for the stimulus DAC only)

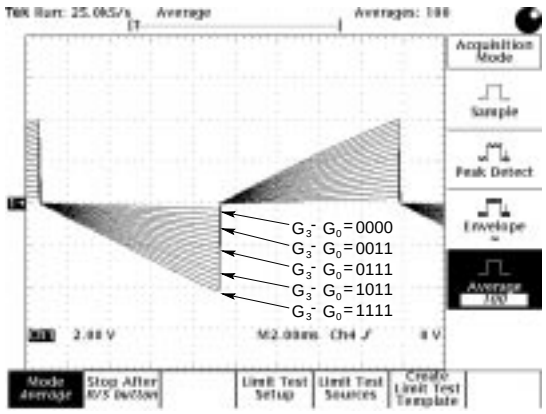


Fig. 8. Experimental measurement of the 4-bit gain prescalar

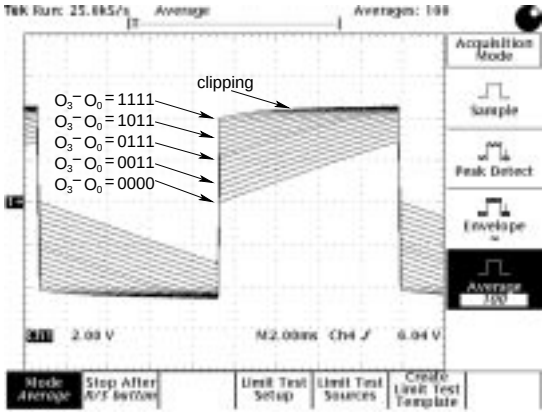


Fig. 9. Experimental measurement of the *multi-bias* DC-offset DAC

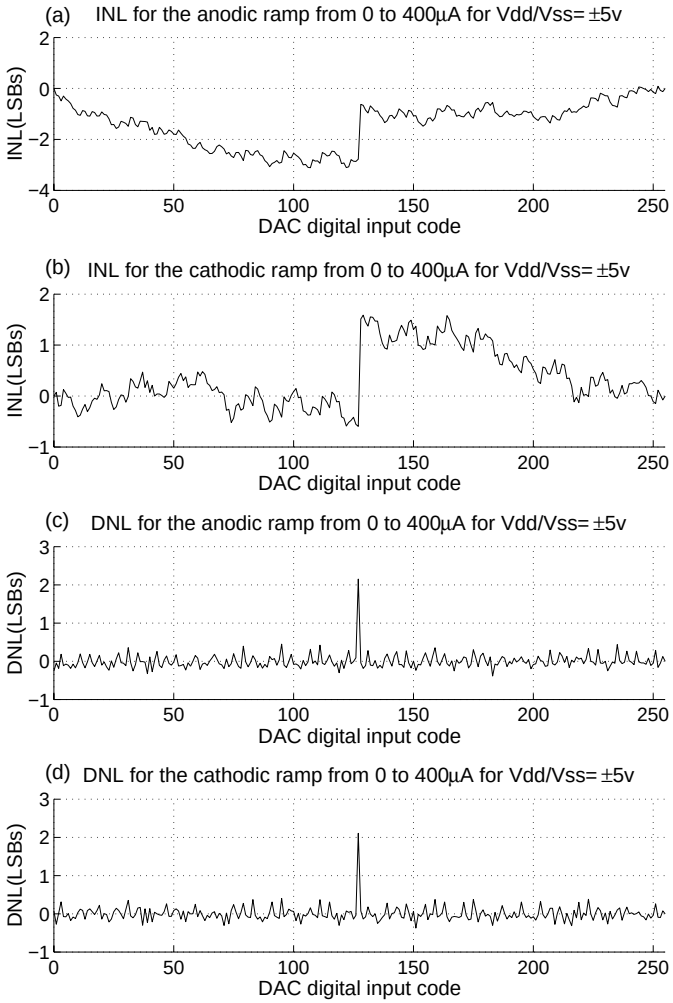


Fig. 10. Experimentally measured integral and differential non-linearity characteristics of current outputs from Figure 4 at $400\mu A$ full-scale for $V_{dd}/V_{ss} = \pm 5$v

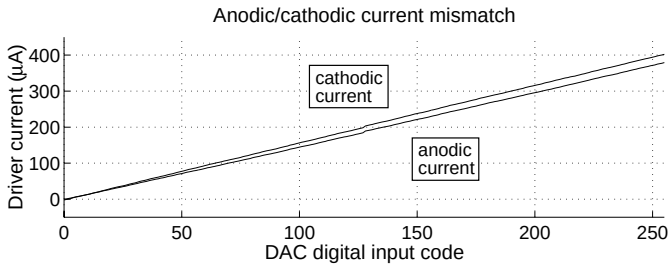


Fig. 11. Experimentally measured current amplitude matching between the anodic and cathodic phases for 400μA full-scale current at $V_{dd}/V_{ss} = \pm$5v

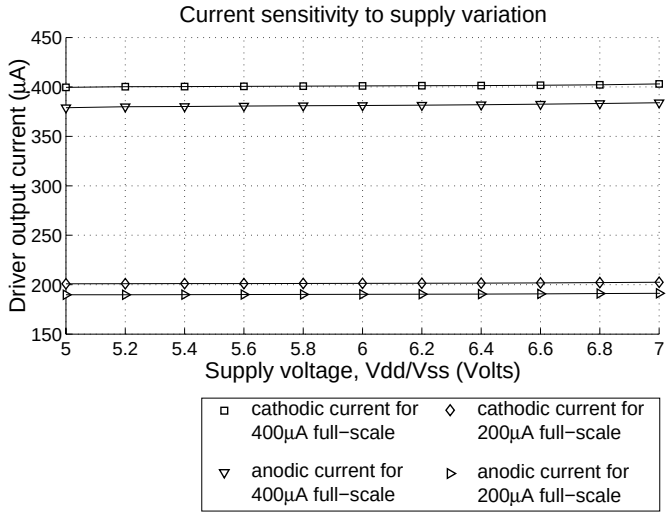


Fig. 12. Experimentally measured current dependence on supply variation

TABLE II

BRANCH CURRENT SENSITIVITY TO BIAS NOISE

bias[1]	nominal value [V_{DC}]	nominal i_{DS}[2] [μA]	Δi_{DS}[3] from +10mV ΔV [nA]	% diff	Δi_{DS}[3] from −10mV ΔV [nA]	% diff
$V_{DbiasS7}$	5.188	10.030	−189.43	−1.89	191.00	1.90
$V_{DbiasS6}$	5.473	5.0270	−138.39	−2.75	140.12	2.79
$V_{DbiasS5}$	5.67	2.5220	−100.19	−3.97	102.06	4.05
$V_{DbiasS4}$	5.806	1.2670	−72.56	−5.72	74.50	5.88
$V_{DbiasS3}$	5.9	0.6379	−52.76	−8.28	54.82	8.60
$V_{DbiasS2}$	5.965	0.3219	−37.57	−11.73	39.94	12.47
$V_{DbiasS1}$	6.011	0.1628	−25.28	−15.61	27.91	17.24
$V_{DbiasS0}$	6.046	0.0823	−15.78	−19.25	18.28	22.30
$V_{DbiasC7}$	3.037	10.030	−5.70	−0.06	5.70	0.06
$V_{DbiasC6}$	3.653	5.0270	−3.86	−0.08	3.84	0.08
$V_{DbiasC5}$	4.078	2.5220	−2.62	−0.10	2.61	0.10
$V_{DbiasC4}$	4.373	1.2670	−1.81	−0.14	1.81	0.14
$V_{DbiasC3}$	4.576	0.6379	−1.27	−0.20	1.27	0.20
$V_{DbiasC2}$	4.716	0.3219	−0.89	−0.28	0.89	0.28
$V_{DbiasC1}$	4.816	0.1628	−0.60	−0.37	0.60	0.37
$V_{DbiasC0}$	4.893	0.0823	−0.38	−0.46	0.38	0.46

[1]Bias potentials correspond to the 8-bit fully cascoded bias generator of Figure 14a set to produce a 20μA full-scale current in the multi-bias DAC of Figure 14b ("S" subscript refers to a current-source bias potential; "C" subscript refers to a cascode bias potential).
[2]Branch current is taken in association with the corresponding bias.
[3]Bias potential is offset $\pm$10mV to model noise.

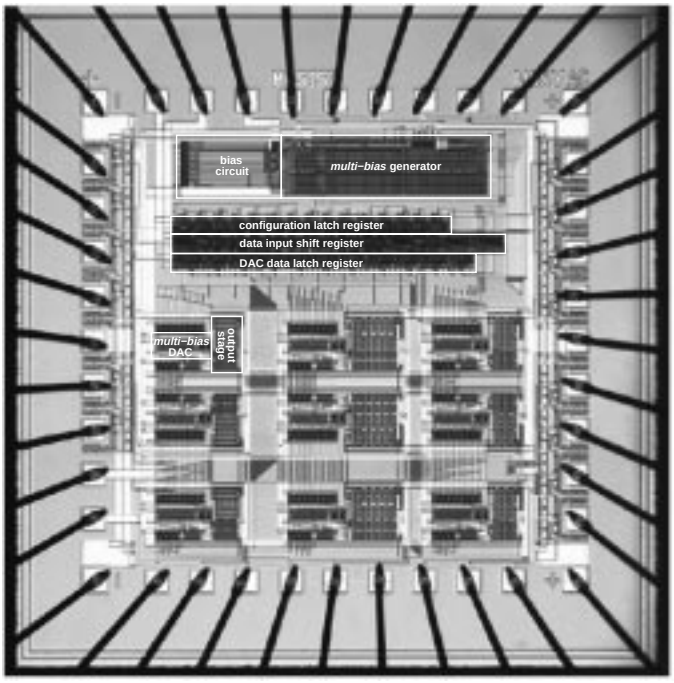
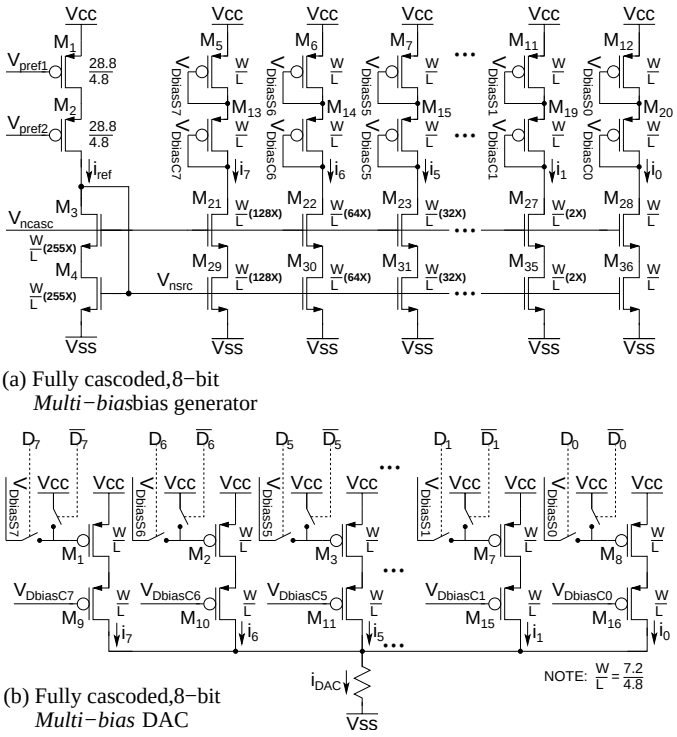


Fig. 13. Die micrograph of the *multi-bias* DAC prototype IC



(a) Fully cascoded,8−bit *Multi−bias*bias generator

(b) Fully cascoded,8−bit *Multi−bias* DAC

Fig. 14. Fully cascoded topology of the *multi-bias* concept

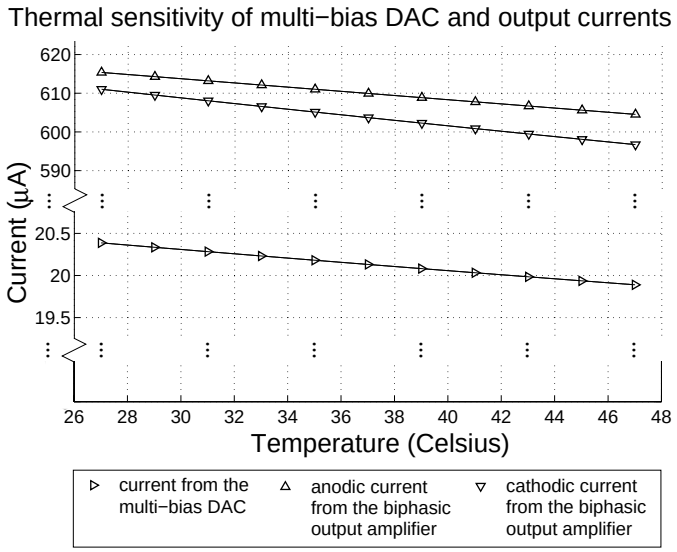


Fig. 15. Thermal dependence of currents from the *multi-bias* DAC and the biphasic current amplifier (simulation data)