A 60 Channel, Implantable Neuro-Stimulator for an Epi-Retinal Visual Prosthesis

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***Abstract*—Retinitis pigmentosa and age-related macular degeneration lead to blindness through progressive loss of retinal photoreceptors. In this paper, we describe a retinal prosthesis system which is designed to compensate for the loss of these photoreceptors for the recovery of some useful vision. The system consists of an extraocular unit and an intraocular unit which are coupled together via a wireless inductive telemetry link. The extraocular unit provides for image acquisition and processing and consists therefore of an external camera, image processor, telemetry encoder, RF amplifier and a primary coil. The intraocular unit receives power and data from the extraocular unit. It consists of a secondary coil, power rectifier and regulator, telemetry decoder, a retinal stimulator chip, and an electrode array. We focus on the design and testing of the implantable microchip which provides electrical stimulation to the post-degenerate retina. It is fabricated through MOSIS in 1.2μm CMOS and provides sixty unmultiplexed biphasic current outputs which can be programmed to influence and affect visual perception in real time.**

***Index Terms*—analog-digital, cmos, mixed-signal, vlsi**

I. Introduction

Age Related Macular Degeneration (AMD) and Retinitis Pigmentosa (RP), among the leading causes of blindness[1], effect over 10 million people worldwide through progressive photoreceptor loss (rod/cones) in the retina [2]. The photoreceptor cells in a healthy retina initiate a neural signal in response to incident light. This neural signal is further processed by bipolar and ganglion cells of the inner retina prior to delivery to higher visual processing areas in the cortex. Retinal photoreceptors are almost completely absent in the retina of end-stage RP and AMD patients, while the bipolar cell and ganglion cells, through which the photoreceptors normally synapse, may survive at higher rates [3]. The ganglion and bipolar cells remain intact, and due to the anatomy of the retina, they are in a position where they may respond to artificially-induced electrical stimulation via an implant. The demonstration that direct electrical stimulation of retinal ganglion cells can create visual sensation in patients has been shown clinically [4]. When stimulated with an array of small retinal electrodes, patients have experienced individual percepts which when viewed collectively produce a visually perceived image consistent with the programmed pattern of stimulus signals on the electrode array. Patients have been able to recognize English characters and other simple patterns when stimulated by a small array of retinal electrodes. This opens the possibility of an electronic prosthesis to bypasses the defective photoreceptors.

The waveform used for electrical stimulation of tissue is the charge-balanced biphasic current pulse shown in Figure 1. The quality and intensity of visual perception can be influenced by variations in amplitude, pulse-width, interpulse-delay, and frequency [4]. The microchip described in this paper is designed to produce these stimulus pulses to be independently programmable remotely by the medical doctors after the microchip has been implanted.

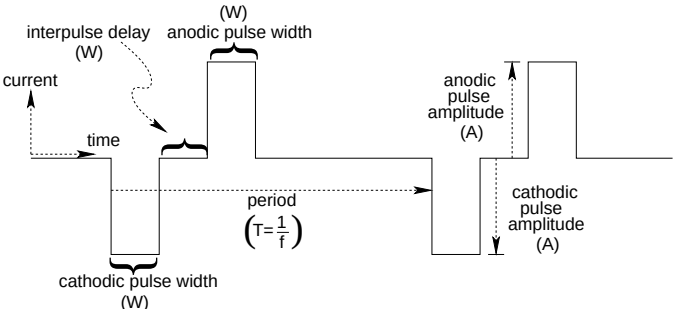

Fig. 1. Parameters of the biphasic current stimulus pulse

Acute medical experiments have determined that the effective impedance of RP and AMD degenerate retinal tissue at the stimulation frequencies of interests (40Hz-60Hz) varies around a value of 10kΩ [5] and could require stimulus currents amplitudes upwards of 600μA [6].

Several other neuro-stimulator devices have been designed and fabricated for electrical stimulation of tissues in vision applications, including epi-retinal [7]-[10] sub-retinal stimulators [11]-[13]. A number of devices provide cortical stimulation and recording [14], [15]. However, most of these do not provide stimulus currents amplitudes at the necessary levels [5], [6]. In addition, the timing constraints on the biphasic currents necessary for retinal stimulation [5], [6] in conjunction with the high electrode counts underscore the need for a design which can stimulate multiple sites concurrently to achieve a image frame rate without flicker perception [5].

Our most recent IC design [16], provides 20 stimulus current driver circuits which are time-division demultiplexed to drive 100 channels. At the loss of some channels, the new design provides 60 stimulation channels which are *unmultiplexed* for greater freedom in scheduling the available channels and increasing throughput *via* the means to stimulate multiple sites concurrently. We have also switched from the bridge-type biphasic driver circuit to a push-pull configuration which is more suitable for the monopolar (common return) electrode configuration, but which can also be used together with neighboring channels in a bipolar or multipolar configuration.

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This paper is divided into six sections. An overview of our prosthesis system is summarized in Section II. The architecture and functionality of the chip are presented in section III, with attention given to circuit design issues. Section IV provides experimental measurements of the chip. Limitations of the device and means of potential design enhancement in future revisions are presented in Section V with the conclusion given in Section VI.

II. Epi-Retinal Prosthesis System

Our prosthesis system design is shown in the block diagram of Figure 2. Dotted lines differentiate extraocular components from the implanted portion, which are coupled together via a wireless inductive telemetry link. The extraocular unit provides for image acquisition and processing and consists therefore of an external camera, image processor, telemetry encoder, RF amplifier and a primary coil. The intraocular unit receives power and data from the extraocular unit. It consists of a secondary coil, power rectifier and regulator, telemetry decoder, a retinal stimulator chip, and an electrode array.

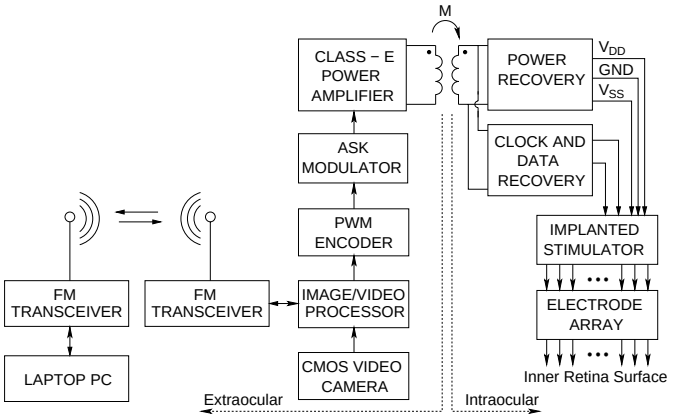

Fig. 2. Proposed system diagram for the retinal prosthesis prototype

The extraocular unit acquires digital images from a mini-camera which are post-processed with external hardware to derive simple stimulus commands for the implant. These instructions correspond to one of two packet types (configuration or image), both of which are ASK/PWM encoded according to the protocol described in [16]. The resulting signal modulates the power carrier output of an RF amplifier which drives the external primary coil. A second implanted coil coupled to the primary coil receives the modulated RF power carrier, from which power and data are recovered using rectifier/regulator and telemetry decoder circuits [16]. The resulting clock and data signals supply the stimulus instructions to the implanted microchip. In this paper, we focus on the design and testing of the block labeled as the "Implanted Stimulator", connecting to the electrode array and providing electrical stimulation to the RP/AMD degenerate retina.

III. Implantable Retinal Stimulator Chip

A. Chip Specifications and Architecture

The block architecture of our chip illustrated in Figure 3 is designed to deliver the programmable biphasic current pulse of Figure 1. About 75% of the IC area is accounted for by the array of sixty stimulus current circuits each of which drives a separate output channel (*ie*- I/O pad). Data for stimulus amplitudes is serially shifted throughout this driver array and latched as implied in the figure and explained in greater detail in Section III-C.

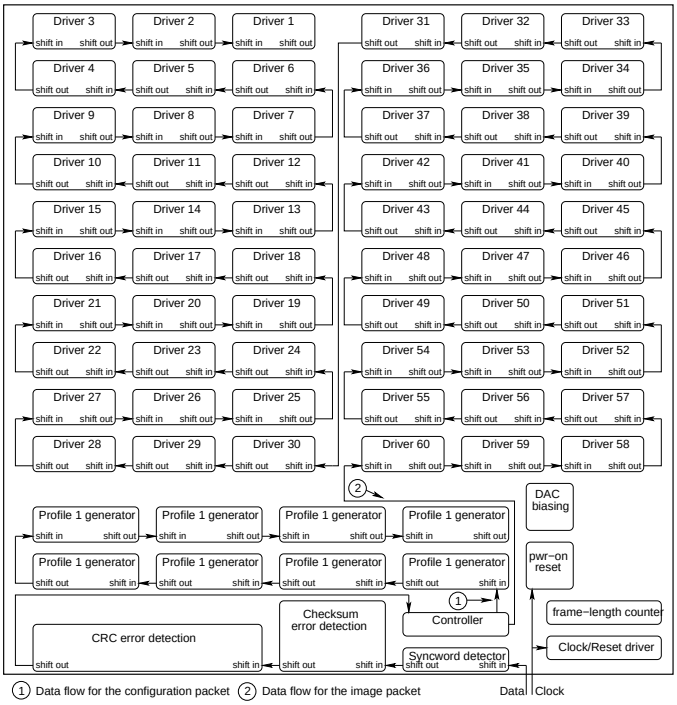

Fig. 3. Architecture of the stimulator microchip

The lower 25% of the chip consists of digital circuits for processing communication packets and for controlling stimulus pulse timing. About half of the lower area is accounted for in the generation of eight pulse timing profiles, each of which is defined by a programmable *start* and *stop* time, relative to the onset of the stimulation frame (*ie*- when an image packet is latched for processing). These timing profiles are generated centrally and distributed to all of the drivers. Each of the sixty stimulus output channels can be programmed to reference one of these timing profiles for its anodic pulse and a second one for its cathodic pulse, thereby providing the means to program pulse widths, interpulse delay, and which phase occurs first in the full biphasic current pulse. The frequency of the biphasic currents pulses (see Figure 1) and therefore the stimulation rate is directly controlled by the clocking rate of data into the chip.

The remaining circuit blocks in Figure 3 consist of the 16-bit data packet synchronization detector, the packet length counter, CRC and checksum circuits for error detection, and the central state-based controller. The implementation of these blocks in discussed in Section III-C.

B. Communication Protocol

Packet information governing the operation of the stimulator is defined digitally and loaded into the chip serially through a *data* input and accompanying *clock* input. A *configuration frame* format is defined for specification of the timing parameters. An additional *image frame* format exists for defining cur-

rent amplitudes in the driver array. Both of the frames are 1024 bits in length.

B.1 Configuration Frame Packet Format

The format of the configuration frame is illustrated in Figure 4a. A unique 16-bit synchronization word identifies the beginning of a configuration frame. Following the sync-word are 830 "don't-care" bits after which are two bits which set the full scale amplitude of the stimulus circuits at 200μA, 400μA, or 600μA, with 4-bit DAC resolution spread uniformly across the selected range. Following this are the start and stop times which of the eight pulse enables (profiles) which define start and stop times for the anodic and cathodic phases of biphasic output currents produced by the sixty drivers. Once the synchronization word for configuration data is detected, the error detection unit is initialized and directed to compute an internal CRC and checksum signature. These are compared against the signatures embedded in the packet. If both signatures match and a correct sync-word is in position for the subsequent packet, then the packet information is transferred into holding registers. This defines the reference time against which the pulse-profile start and stop times are internally measured.

B.2 Image Frame Packet Format

The format of the image frame is illustrated in Figure 4b. It is also initiated with a unique 16-bit sync-word word, after which are sixty 16-bit driver data-words formatted as shown in the inset of Figure 4b.

The most significant bit (bit-15) is unused. The cathodic and anodic references select one of the eight pulse timing profiles, where any pair-wise combination of the profiles can be specified for each of the sixty drivers. The cathodic/anodic cathodic amplitude specifies the current level (relative to the full-scale current specified in the configuration data) to produce during the cathodic/anodic phase. Bit 7 of the driver data-word controls the charge cancellation facility. In order for the chip to produce a correct biphasic pulse, anodic and cathodic phases and the charge cancellation duration should not overlap in time. The image packet ends with embedded CRC and checksum signatures for error detection. As before, if both signatures match and the follow-on sync-word is recognized, then all sixty driver data-words from the image packet are latched into appropriate holding registers in the driver array. Otherwise, the data is ignored and overwritten as new packets arrive.

B.3 Communication Synchronization

The possibility of a drop bit(s) in communication with the implant requires monitoring synchronization with the chip. This is accomplished by checking that the sync-word appears at the beginning of each frame. The 10-bit frame length counter is initialized as the sync-word is detected. As it reaches its final value and signals the end of the packet, the sync-word for the following packet should already be shifted into the chip and be in the correction position to confirm the onset of a new packet. If it does not appear on schedule, then the chip continues to shift in new packets but stops latching packets until a sync-word is re-acquired.

B.4 Detection and Treatment of Communication Errors

Robust communication is strengthened by the 32-bit CRC and a 16-bit checksum computations. Packets invalidated by dropped or erroneous bits should yield CRC and checksum computations with a high probability of being inconsistent with the signatures provided in the packet. Unambiguous actions are defined to maintain correct chip behavior for errors in configuration and image packets and the dependencies between them. If packet synchronization is lost at any time, then the controller returns to an initial state and waits to re-acquire packet sync. The chip will not process any image packets until a configuration frame has first been received without error and latched.

C. Circuit Design

C.1 Timing Profile Generator Design

The profile generators produce the eight digital timing signals for the current drivers according to the eight 8-bit start-time/stop-time pairs programmed in the configuration packet. Each time parameter represents a count of clock-cycles in multiples of four, relative to the latching of each of image frame. Accordingly, edge placement has a resolution of 1/256 of the frame time, or equivalently four periods of the input clock. A diagram of the pulse timing profile subsystem is provided in Figure 5a.

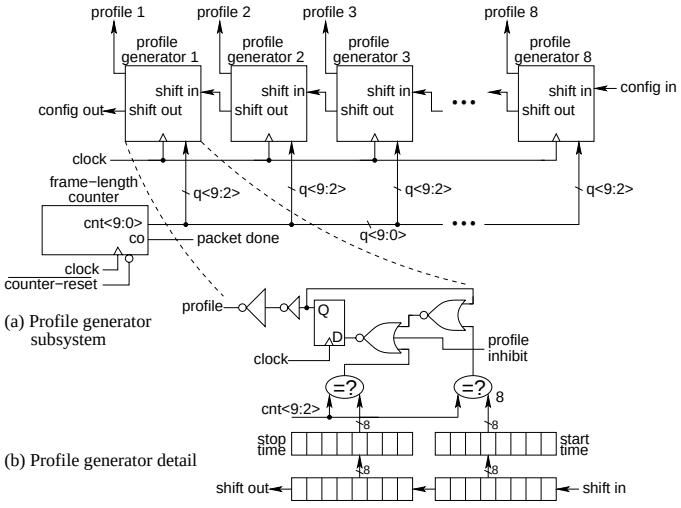

Fig. 5. Pulse timing profile generator subsystem

The start and stop time parameters are shifted in from the configuration packet and latched into holding registers. The 10-bit frame length counter is cleared to zero upon the detection of a packet sync-word and then begins incrementing. The upper 8-bits of the 10-bit frame-length counter are compared with the *start* and *stop* times stored within each pulse-profile generator. Once the *start* time is reach the pulse-profile is asserted *high*. As the *stop* time is reached, the pulse-profile is returned *low*. This occurs in parallel for the eight profile generators, as shown in Figure 5a. The detail of each profile generator is given in the inset of Figure 5b.

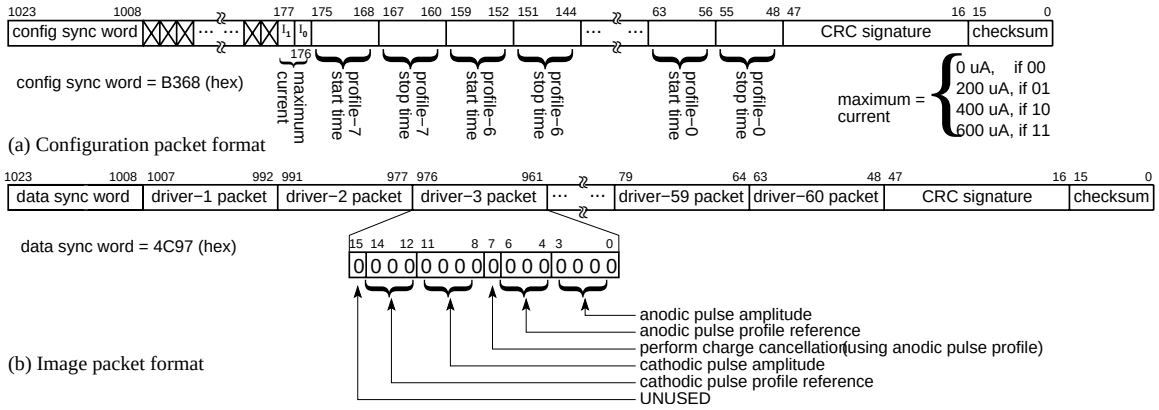

Fig. 4. Packet format definitions for the stimulator IC

C.2 DAC circuit

The stimulus driver circuit employs two 4-bit NMOS binary-weighted current-mode DACs to produce the anodic and cathodic currents. The DAC design, shown in Figure 6, is designed with wide-swing cascode current mirrors referenced to V_{ss} in which the LSB branch current subcircuits are duplicated $2\times$, $4\times$ and $8\times$ to implement the binary weighting with respect to the digital input code, D_3-D_0. The cascode NFETs M_1-M_4 are biased directly from the signal *dcas*, generated in the bias circuit. The current source NFETs M_5-M_8 have their gates switchable to either *ibias*, generated in the bias circuit (yielding the ON state) or to V_{ss} (for the OFF state). This occurs under control of the digital input code, D_3-D_0 (supplied by the image frame). The requested current amplitude specified by D_3-D_0 is gated by the *profile* signal selected from one of the eight pulse profile generator outputs (Figure 5a and Figure 5b), such that the DAC current is enabled only while the timing profile signal is asserted.

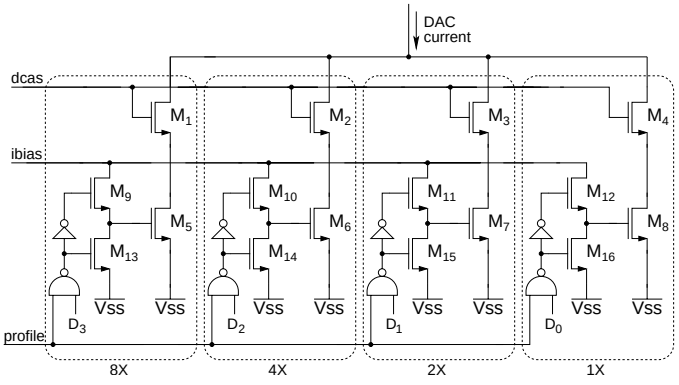

Fig. 6. Current mode DAC circuit detail

C.3 Biphasic Current Amplifier

Experimental measurements on RP degenerate retina indicate that it presents roughly 10kΩ of impedance to the driver circuits [5], which for 600μA currents produces 6v drop across the combined electrode/retina impedance. This will require supply rails for the stimulus circuits that are higher that $\pm$6v and could eventually require transistor structures which can support high drain-source voltages [17]. In the interim, the stacked PMOS-DAC/NMOS-DAC arrangement [14], [15] conducive for smaller currents is modified so that the DACs produce reduced currents at lower voltage levels, which can be mirrored and scaled into a higher voltage compliant output circuit. The circuit for this is shown Figure 7. The current mirrors are wide-swing cascoded to achieve the lowest V_{dd}/V_{ss} supplies, presently set to $\pm$7v. Anodic current is sourced from V_{dd} to the tissue impedance with $10\times$ gain through PFETs M_{17} and M_{18}. Cathodic current is sinked from the load to V_{ss} through NFETs M_{19} and M_{20}, also with $10\times$ gain.

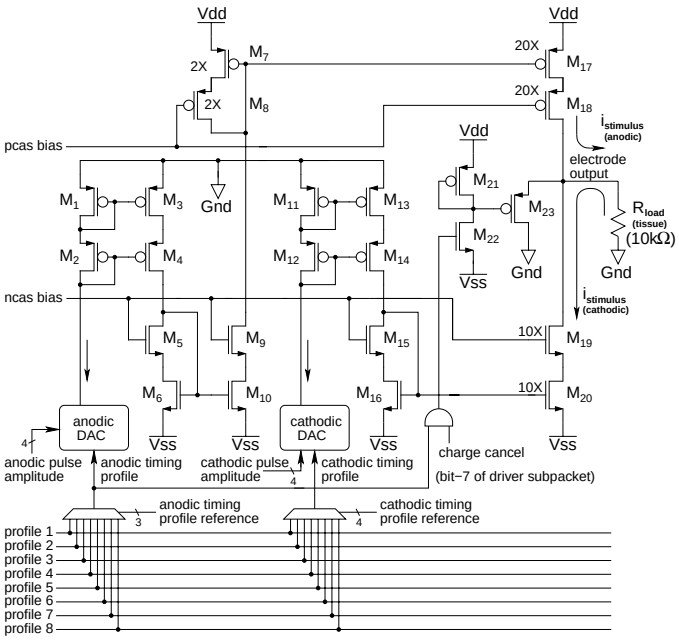

Fig. 7. Circuit level detail of the biphasic amplifier in the current driver

In addition to the DACs, each current driver contains two 8-to-1 multiplexors to select from among the timing profiles. The final component of the driver circuit is a charge cancellation mechanism, which is intended to limit any unintentional accumulation of charge on the electrode. This circuit functions by shorting the electrode to the ground return through PFET M_{23}.

C.4 Biasing circuit

The wide-swing cascode current mirrors in the NMOS DACs and the biphasic amplifier stage receive their bias voltages from a central biasing circuit [16], shown in Figure 8, which are then distributed throughout the driver array. The biasing circuit can be considered in three sections.

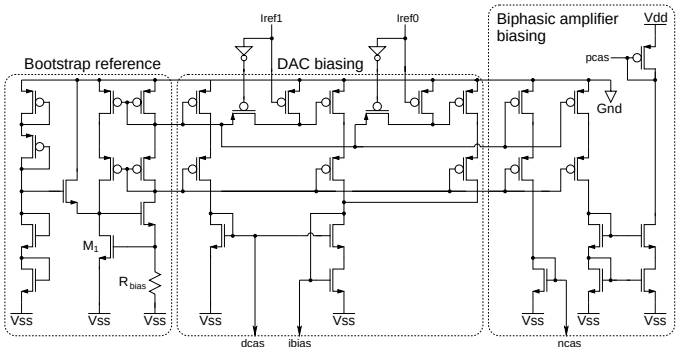

Fig. 8. Central bias circuit for the DACs and the biphasic amplifiers

The *bootstrap reference* achieves a 20μA master reference current. The *DAC biasing* section taps the cascode current mirror in the bootstrap reference to establish the two biases *dcas* and *ibias* (see Figure 6) for the DACs in the drivers circuits. Using the two bits $Iref_1$ and $Iref_0$ from a latched configuration packet (see Figure 4a), the DAC biasing section can be tuned to mirror the master reference current with gains of $1\times$, $2\times$, or $3\times$ permitting full-scale stimulus current amplitudes of 200μA, 400μA, or 600μA. The *Biphasic amplifier biasing* section provides the NMOS and PMOS wide-swing cascode biases *ncas* and *pcas* for the driver output stage of Figure 7.

IV. Measurement Results

A. Waveform Versatility

Experimentally measured biphasic stimulus current output generated simultaneously from four different driver circuits is shown in Figure 9. The circuits were loaded with 10kΩ which is the the nominal retinal impedance [5]. Initially we considered V_{dd}/V_{ss}=$\pm$5v since these are the nominal supplies for this 1.2μm IC process. Accordingly, the drivers were programmed to deliver the maximum output current (D_3-D_0=1111 in Figure 6) at the 400μA full-scale current setting ($Iref_1$=1, $Iref_0$=0 in Figure 8). The waveforms represent voltage measurement across the load. These plots show the versatility of the chip to produce biphasic stimulus currents with independently programmable pulse widths in the anodic and cathodic phases (waveforms 1-3) as well as to adjust the interpulse delay, even down to zero (waveform 4). Also, illustrated in the bottom waveform is the means to assign an anodic-leading or cathodic leading pulse. The chip clock frequency was set to yield a stimulation frame rate of 300 pulses/second.

B. Accuracy and Linearity

Figure 10 shows experimentally measured current amplitude from a single driver circuit connected to a 10kΩ load, plotted as a function of the DAC digital input code (D_3-D_0 in Figure 6).

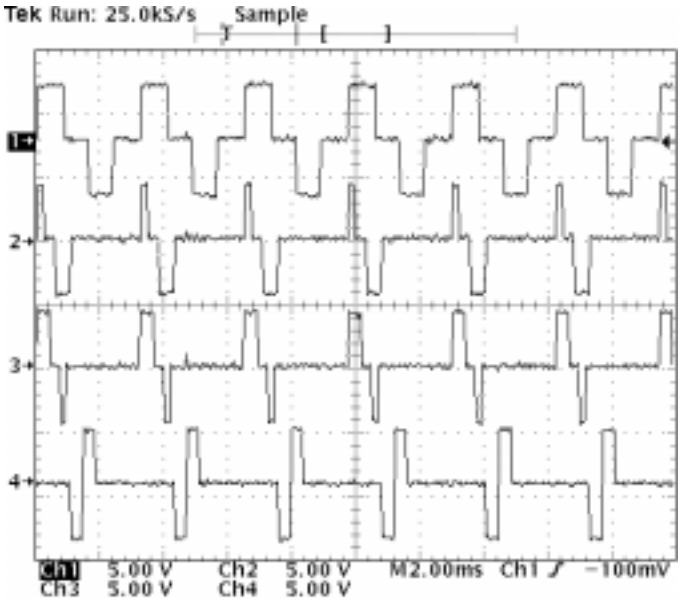

Fig. 9. Experimentally measured biphasic stimulus currents waveforms

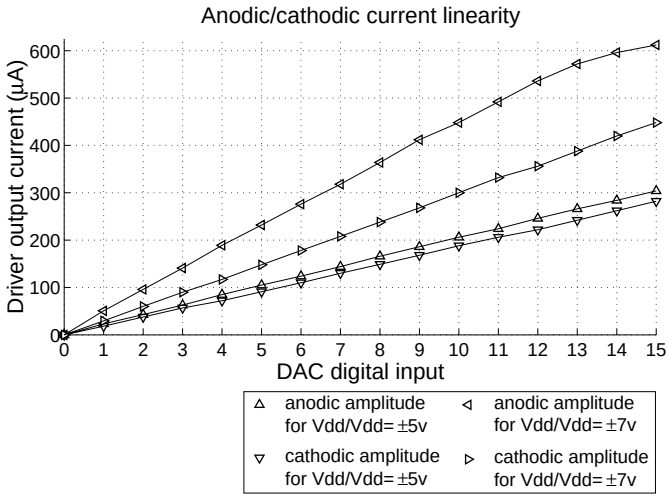

Fig. 10. Experimentally measured anodic and cathodic current amplitudes vs. DAC digital input for $V_{dd}/V_{ss} = \pm$5v and $V_{dd}/V_{ss} = \pm$7v.

Once again we initially consider V_{dd}/V_{ss}=$\pm$5v which is the optimal supply level for this IC process. Accordingly, the full-scale current level of 400μA is programmed ($Iref_1$=1,$Iref_0$=0 in Figure 8). The data shows that the maximum stimulation current associated with D_3-D_0=1111 is less than the 400μA target value with the shortcoming common to both the anodic and cathodic current magnitudes. This points to an offset in the desired reference current in the bias circuit, owing to process variation in the fabrication of the linear resistance in Figure 8.

We also measure the linearity of the stimulus current magnitude versus DAC input, since this is a desirable feature in characterizing the effectiveness of electrical stimulation on visual perception. We consider the end-point INL estimate given by the sum of the DNL errors for which the anodic and cathodic currents at $V_{dd}/V_{ss} = \pm$5v in Figure 10 evaluates to 0.8224 and 0.8085, respectively, where INL for the ideal straight line is zero. The tracking between the anodic and cathodic amplitudes

exhibits an error that increases with the current magnitude, pointing to a static gain mismatch between the PMOS sourcing and NFET sinking circuits of Figure 7. At D_3-D_0=1111, the tracking error is 7.24% with respect to the anodic current. The charge imbalance introduced by this mismatch can be neutralized with the charge cancellation facility, discussed in Section IV-D.

Overlayed onto Figure 10 are similar measurements where the supply rails are extended to V_{dd}/V_{ss}=±7v to support the delivery of 600μA full-scale current ($Iref_1$=1, $Iref_0$=1) to the 10kΩ load. Here again, we estimate the INL of the anodic and cathodic phases to be 2.5098 and 0.7277, respectively. The nonlinearity estimate for the anodic current is higher owing to the trailing off of output current approaching D_3-D_0=1111, where PFETs M_{17} and M_{18} in Figure 7 enter the linear region as the increasing load voltage reduces V_{ds} for these FETs. The anodic to cathodic tracking at V_{dd}/V_{ss}=±7v is much worse, exhibiting a percent difference of 26.80% at maximum DAC output current. The reason for this anomalous behavior is not solely a reduced cathodic current as it might appear. Figure 10 shows that both current phases are lower that the targeted values for both the $V_{dd}/V_{ss} = \pm$5v and $V_{dd}/V_{ss} = \pm$7v supply levels.

The cause of the large mismatch is actually a higher anodic current than should occur with respect to the cathodic current, owing to channel breakdown in the transistor due to high V_{ds}. In Figure 7, M_7 and M_8 are wide swing connected and the gate of M_9 is connected to a constant potential, *ncas bias*. Thus, the voltage appearing at V_{ds} of M_9 is $V_{dd} - V_{ss} - (V_{ncas\_bias} - V_{gs9}) - |V_{gs7}|$ and hence any increase in V_{dd}/V_{ss} directly increments V_{ds} of M_9. High V_{ds} in a transistor results in high electric field in the channel, which imparts excessive energy to the channel electrons especially near the drain region. These high energy electrons generate electron-hole pairs due to impact ionization. The holes are attracted to the negatively biased bulk where they appear as a substrate current. The associated electrons from the electron-hole pairs increase the drain current in M_9 [18]. This excessive drain current tracks in M_7 and M_8 and is reflected in the anodic current.

C. Power Supply Variation

When the chip is powered with a wireless inductive telemetry link, it can experience DC supply variations from relative movement between the coils. As we noted in our prior paper [16], this can modulate the amplitude of the output stimulus currents directly by offsetting V_{ds} in the current source FETs of Figure 7 and indirectly by offsetting V_{gs} in these FETs through a shift in the reference current. The latter is dealt with via a bias circuit exhibiting low sensitivity to supply variation as does the design of Figure 8. The former concern is addressed with high impedance current mirrors which we employed in Figure 7. We quantify in Figure 11, the chip's immunity to supply variation over a range of $\pm$4v $\leq V_{dd}/V_{ss} \leq \pm$7v over the three selectable current ranges of 200μA, 400μA, and 600μA. Supplies of V_{dd}/V_{ss}=±7v are nominal for 600μA currents into 10kΩ loads, but this already stresses the gate oxides, so we did not push the supplies beyond these values in Figure 11.

The waveforms highlight the channel breakdown effect [18] in the anodic currents as we discussed in Section IV-B, which

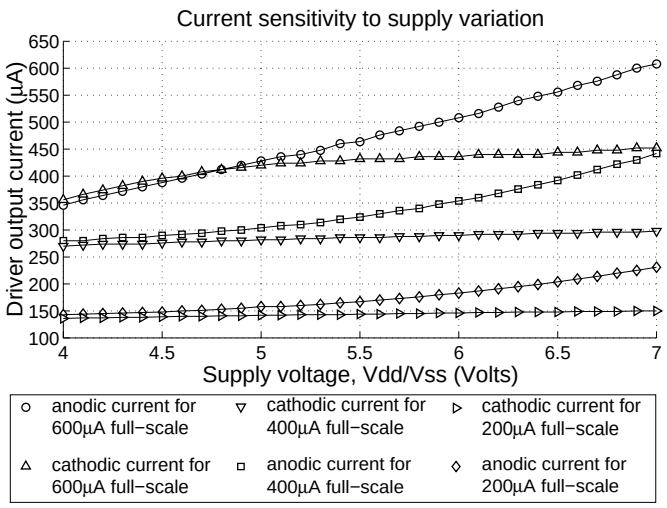

Fig. 11. Experimentally measured stimulus current amplitude sensitivity to power supply variation

begins to take effect beyond V_{dd}/V_{ss}=±5v. Therefore, it is from the cathodic currents that we assess supply variation immunity for the chip. We see that in the highest selectable current range of 600μA range that the reduced cathodic current can be supported down to V_{dd}/V_{ss}=±5v at which point the driver circuit loses the headroom to keep its current mirrors saturated. Apart from the shift in the measured bias current, the cathodic current would be nearer to 600μA with minimum needed supply rails of V_{dd}/V_{ss}=±7v. Over the domain of $\pm$5v $\leq V_{dd}/V_{ss} \leq \pm$7v, the cathodic current in the 600μA setting shows good immunity to supply variation with a measured dependence of 16μA/V. Likewise, the cathodic currents in the 200μA and 400μA ranges also show good immunity over $\pm$4v $\leq V_{dd}/V_{ss} \leq \pm$7v with measured dependences of 9.33% (4.66μA/V and 9.33μA/V, respectively).

D. Charge cancellation

The charge cancellation feature in the chip can be selectively programmed per driver circuit to deplete any accumulating charge on the output electrode. In order to emulate the effect of stray charge during idle time, the nominal R_{load}=10kΩ resistance used to model tissue impedance at around 60Hz stimulation [5] is replaced with a discrete capacitance, $C_{load} = 274$nF, approximately the same impedance at 60Hz. Figure 12 shows linear charging during the anodic current phase and linear discharging during the cathodic phase. A charge balanced biphasic current would cause the load voltage to return to zero. Here, an anodic current of 300μA and a cathodic current of 150μA leads to non-symmetric charging of the load with excess charge remaining on the load capacitance during the idle time, which must be depleted. The bottom waveform in Figure 12 indicates the assertion of a programmed charge cancellation pulse. This leads to an R-C discharge of the load capacitance through the resistance of M_{23}. From the time constant of the decay, PFET M_{23} is estimated to have resistance of 13kΩ. The duration of the charge cancellation enable pulse must be sufficiently long to affect a complete removal of the charge on the electrode, which is indicated as the output voltage returns to zero prior to the onset of a subsequent stimulation current pulse. We have used

TABLE I

Hspice SIMULATED POWER DISSIPATION IN THE PROTOTYPE IC RESULTING FROM VARIATIONS IN BIPHASIC STIMULUS CURRENT PULSES

V_{dd}, V_{ss} $[V_{DC}]$	current A $[\mu A]$	frame rate $f=\frac{1}{T}$ [Hz]	pulse width W [ms]	bias power P_{bias} [mW]	digital power $P_{digital}$ [mW]	driver power×60 $P_{driver}\times 60$ [mW]	load power×60 $P_{load}\times 60$ [mW]	simulated chip power[1] P_{chip} [mW]	measured chip power[1] P_{chip} [mW]
+5, −5	400	50	1	2.4700	0.4726	6.2436	9.8004	9.1862	7.1541
+5, −5	400	50	2	2.4700	0.4726	12.2154	19.5066	15.1580	15.6219
+5, −5	400	50	3	2.4700	0.4726	18.2448	29.3070	21.1874	24.3513
+5, −5	400	60	1	2.4700	0.4750	7.4562	11.7030	10.4012	10.7877
+5, −5	400	60	2	2.4700	0.4750	14.6568	23.4066	17.6018	19.9302
+5, −5	400	60	3	2.4700	0.4750	21.8568	35.1102	24.8018	27.6076
+7, −7	600	50	1	3.5647	0.4964	12.2604	19.8618	16.3216	–[2]
+7, −7	600	50	2	3.5647	0.4964	23.7696	39.5310	27.8308	–[2]
+7, −7	600	50	3	3.5647	0.4964	35.3916	59.3928	39.4527	–[2]
+7, −7	600	60	1	3.5647	0.5017	14.6448	23.7174	18.7112	–[2]
+7, −7	600	60	2	3.5647	0.5017	28.5228	47.4354	32.5892	–[2]
+7, −7	600	60	3	3.5647	0.5017	42.4008	71.1540	46.4672	–[2]

[1]Excludes load power dissipated in R_{load}. $P_{chip} = P_{bias} + P_{digital} + (P_{driver} \times 60)$

[2]Only the cases for V_{dd}/V_{ss}=±5v were considered in the experimental measurement because of the channel breakdown effect discussed earlier occurring at V_{dd}/V_{ss}=±7v, which was not predicted in simulation.

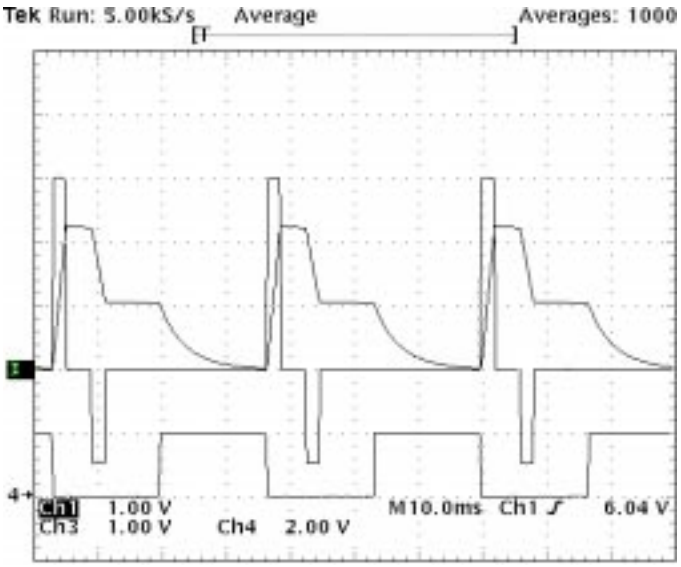

Fig. 12. Experimentally measured operation of the charge cancellation mechanism

TABLE II

CHIP PERFORMANCE SPECIFICATION AND MEASUREMENTS

Technology	MOSIS 1.2μm CMOS
Die size	5.5mm × 5.25mm
Number of current generators	60
Number of electrodes	60
Maximum clock rate	1.5 MHz
Maximum frame rate	1465 frames/sec
Frame size	1024 bits
Amplitude resolution	4-bits, 3 full scale settings
Timing resolution (edge placement)	4 clock cycles, or 1/256 of the frame time
Power consumption	50mW
Anodic current nonlinearity (INL)	0.8224
Cathodic current nonlinearity (INL)	0.8085
Anodic/Cathodic tracking	7.24%
Supply sensitivity	9.33%

16.6ms, the full frame time at 60Hz stimulation rate. Since the chip does not support a biphasic stimulus pulse and charge cancellation scheduled together within a single frame, usage of a full frame time for charge cancellation following a stimulation frame offers the greatest time duration for charge depletion to take place.

E. Power Consumption

Power consumption of the implanted system is accounted for in the chip and in retinal tissue, with the values dependent on the waveform parameters from Figure 1. In Table I, we summarize from circuit simulation the power consumption for several variations in the waveform parameters representing typical usage of the chip as a retinal stimulator [5], [6]. The summary is given for the bias circuit, power in the digital control circuits, and power in the driver circuits and loads, with all 60 output channels simultaneously active. Total chip power the sum of the three components (excluding load power), with an experimental measurement for validation in the rightmost column showing good agreement with the simulated values. Only the cases for V_{dd}/V_{ss}=±5v were considered in the measurement because of the channel breakdown effect discussed earlier occurring at V_{dd}/V_{ss}=±7v, which was not predicted in simulation. Therefore, typical usage the chip is expected to consume under 50mW.

The chip was fabricated through MOSIS in the AMI-1.2μm CMOS process with physical dimensions of 5.5mm × 5.25mm. A die photograph shown in Figure 13 with a summary of experimental measurements given in Table II.

V. DESIGN ENHANCEMENTS

Two changes to the driver circuit of Figure 7 are proposed to enhance its performance for generating biphasic currents. The mismatch at $V_{dd}/V_{ss} = \pm 7$v in Figure 10 resulting from channel breakdown can be eliminated by reducing the voltage drop across M_9 and M_{10}, by placing a number of diode-connected

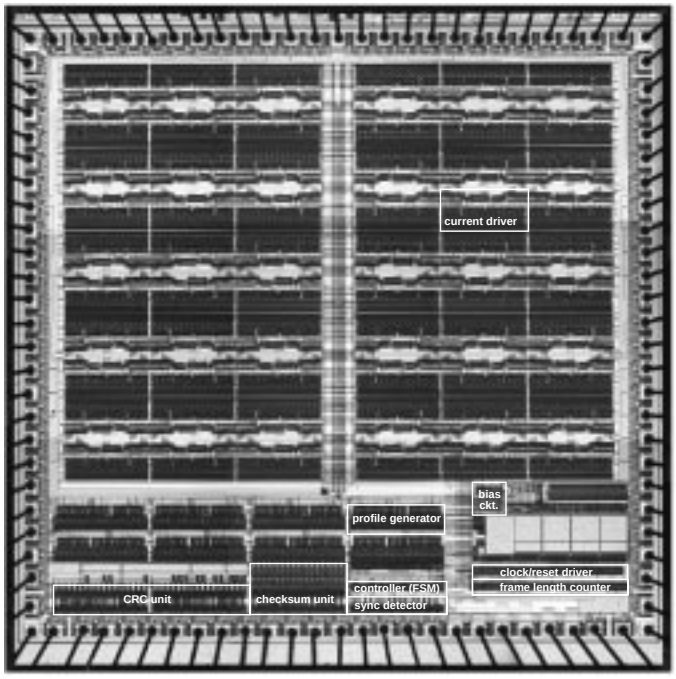

Fig. 13. Die photograph of the prototype stimulator microchip

NFETs between M_8 and M_9 to absorb some of the voltage drop. This will not increase power dissipation since the voltage across and current through the stack is unchanged. Secondly, anodic and cathodic currents derived from one DAC will match better than currents derived from identical yet separate DACs. Accordingly, we propose to combine the two separate DACs of Figure 7 into a single DAC with a multiplexed input, whose current output can be routed via current mirrors to either the M_{17}/M_{18} pair or the M_{19}/M_{20} pair.

Due to constraints on chip area, the ASK and PWM demodulator from our previous IC [16] were not placed on this prototype chip. However, it is planned to integrate these circuits in the next IC revision along with carrier envelope extraction for wireless clock/data recovery and on-chip DC supply generation.

Low resolution vision studies [19] indicate that a visual prosthesis may need to offer more than 60 output channels as in our prototype chip. Circuit enhancements in subsequent IC revisions will seek to obtain higher spatial resolution in a similar die area, while preserving the means to provide 600μA currents to 10kΩ loads.

The bias circuit of Figure 8 produced a lower than expected reference current because the linear resistance was fabricated at a higher value than designed. We propose to improve upon this by employing a digital resistance which can be programmed via a small set of unused data bits in the configuration packet format of Figure 4a, thereby offering the means to tune out process variation, or even to globally adjust output currents beyond 600μA subject to the limits of the supply rails [20].

With the existing charge cancellation circuitry, a programmed depletion event is gated to occur during the anodic pulse timing profile and therefore cannot be concurrent with a biphasic stimulus pulse. A charge cancellation event must occupy an idle frame and if programmed to occur following every stimulation pulse will cut the achievable frame rate in half. We can improve upon this by dedicating one of the eight timing profiles to enable charge cancellation such that it does not overlap in time with the biphasic pulse. This would allow charge depletion to be occur in the same frame time with biphasic stimulus pulse.

VI. Conclusion

The design of our latest implantable microstimulator has been presented for use in an epi-retinal prosthesis. It is programmable in real-time from external hardware via clock and data inputs according to configuration and image data provided in packets at frame-rates up to several hundred images/sec. Sixty unmultiplexed stimulus driver circuits can be programmed with independent pulse amplitudes to represent pixel intensities consistent with acquired image data from an external minicamera. Shared pulse timing parameters are also programmable in the prototype IC. Error detection mechanisms are implemented on-chip to strengthen robust communication of stimulus instructions. The stimulator is designed and implemented in AMI-1.2μm CMOS through MOSIS. Test results show that the driver circuits can produce biphasic stimulus current pulses with some shortcomings which can be easily corrected in subsequent IC revisions in order to become fully compliant with the specifications for retinal stimulation.

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