

AN IMPLANTABLE POWER AND DATA RECEIVER AND NEURO-STIMULUS CHIP FOR A RETINAL PROSTHESIS SYSTEM

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Abstract

In certain diseases of the retina, the photoreceptor cells do not respond to light and thus cause blindness. We describe an electronic retinal prosthesis system that can provide some vision to patients by direct electrical stimulation of the retinal neurons. Power and image data are transferred to the implanted stimulator through a wireless inductive link. The system consists of an external video camera with image processing and encoding hardware and a power and data transmitter. Implanted in the eye are power and data receivers, stimulus circuits, and electrode array. The most recent prototype implant device, implemented in 1.2 micron CMOS, implements demodulation and decoding of the data stream and produces the biphasic current stimulus pulses for an array of 100 retinal electrodes at video frame rates.

1 Introduction

Retinitis pigmentosa and *macular degeneration* are diseases which cause blindness by damaging the photoreceptor cells of the retina (rods and cones) so that they fail to initiate neural signals in response to light. These conditions affect several million people worldwide. However, the demonstration that direct electrical stimulation of retinal neurons can create visual sensation in patients creates the possibility of an electronic prosthesis which bypasses the defective photoreceptors. Volunteers already have been able to recognize English characters and other simple forms when stimulated by small arrays of retinal electrodes [1].

We are developing a prosthetic system illustrated conceptually in Fig. 1. It includes an external camera with data and power transmission circuits mounted on glasses, and implanted receiver and stimulus circuits. The prototype system is intended to achieve two primary goals. First, it will serve as a flexible waveform generator to allow experimental optimization of stimulus waveforms. Second, it will demonstrate wireless transfer of power and data to the implanted stimu-

lator.

In the following, we first describe the architecture of the system, and then focus in more detail on several subsystems. Finally, we present results of early measurements taken on a prototype data receiver and neural stimulator, implemented in 1.2 μm CMOS, which can drive a 10 by 10 array of retinal electrodes at real-time video rates.

2 System Architecture

Fig. 2 shows a functional block diagram of the retinal prosthesis system. A miniature video camera supplies visual information to an FPGA-based image processing unit. The processor collects, compresses, and formats the data for the implanted stimulator. It also can be programmed to implement arbitrary image processing algorithms to enhance the perception of the patient. The processor produces a serial data stream and clock which are encoded as a pulse width modulated (PWM) waveform. The PWM signal is used to amplitude modulate (ASK) a resonant class E amplifier that drives the primary coil of the inductively coupled link. The above components are mounted on glasses to be worn by the patient.

Implanted in the eyeball are the secondary coil, power and data recovery components, stimulus circuits, and the electrode array. The signal produced by the secondary coil is rectified and filtered to produce a DC supply voltage for the implanted circuits. In parallel, the ASK demodulator extracts the PWM waveform from the rectifier output. A decoding circuit then recovers the data and clock signals. The data controls and provides visual information for the stimulus circuits that drive the array of retinal electrodes.

In the current prototype system, the ASK demodulator, data recovery, control logic and stimulator circuits for 100 electrodes are integrated in a single CMOS chip. Future chips will incorporate power recovery and drive larger numbers of electrodes. Several schemes for positioning and connecting to the electrodes are being investigated, such as flex-

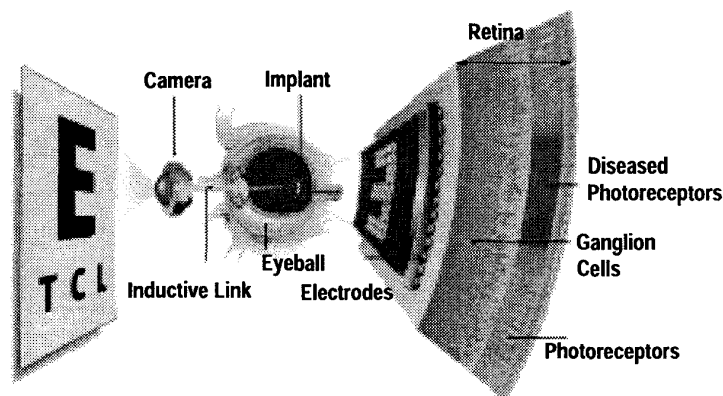


Figure 1: A Retinal Prosthesis

ible polyimide substrates, or growing electrodes directly on the CMOS die.

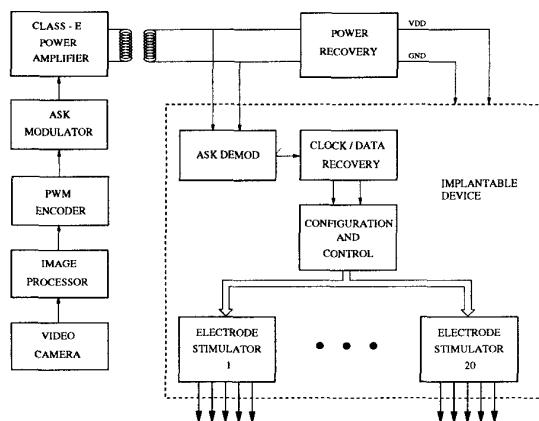


Figure 2: Functional Diagram of the Prosthesis

3 Inductive Power and Data Link

It is medically infeasible to have permanent wired connections pass through the eyeball wall, and so both power and data must be transferred to the implanted circuits through a wireless link. Our system relies on inductive coupling because it can be made efficient despite weak coupling characteristics and it can be implemented with relatively simple circuits.

Power is transferred to the implant simply by DC to AC conversion, magnetic coupling, and AC to DC conversion. Since only a small fraction of the magnetic field in the primary coil couples to the secondary, the uncoupled energy must be recycled rather than dissipated. The resonant class E amplifier topology originally was conceived for such weak coupling situations, and it fits our requirements well. Our

system is designed to operate at frequencies of about 1 to 10 MHz.

Data is transferred by modulating the magnetic “carrier” that couples through the coils. The prosthesis system uses amplitude modulation because it is simple to create in the class E amplifier, and easy to detect in the implant. However, directly controlling the amplitude with NRZ data causes the recovered voltage level to vary with the data values. We eliminate this data dependency by encoding the data in a PWM waveform with a constant average value. The PWM signal then controls carrier amplitude. The system operates with a data rate (PWM frequency) of 30 to 500 KHz. In the following sections, we describe the ASK demodulator and PWM decoder circuits used in the implant device.

The ASK demodulator recovers the digital PWM waveform from the envelope of the inductively coupled ASK waveform. The envelope is obtained by rectifying and low-pass filtering the output of the receiving coil. The filter bandwidth is chosen to suppress the carrier while passing the PWM envelope (the supply voltage is further filtered to a lower bandwidth). The demodulator detects amplitude shifts in the envelope by comparing it to an averaged version [2]. The averaging is performed with an integrated 10 pF capacitor. The comparator circuit implements roughly 1 V of hysteresis [3] to prevent the creation of false transitions in the PWM output by noise or residual ripple.

There are a number of ways to encode a data stream so that the average is roughly constant and thus independent of the particular data values, such as Manchester and 8-bit/10-bit coding. For the retinal prosthesis, we devised a scheme which encodes the data in a digital clock signal with three possible duty cycles. A zero is encoded as a 50 % duty cycle, and a one is $50 \pm \Delta \%$, alternately. This PWM waveform has the additional advantage that the rising edge explicitly provides the clock.

The data stream is recovered from the PWM waveform by a delay-locked loop circuit illustrated in Fig. 3. The DLL locks its voltage controlled delay line (VCDL) to the clock period defined by the rising edge of the PWM waveform.

On each cycle, a small logic block determines in which of three VCDL regions the falling edge resides. The center region, between approximately 40 and 60 percent of the clock period, encodes a zero, and the two outer regions a one. This data recovery scheme is simple to implement, yet it can operate over a wide range of frequencies and in fact can track changing data rates.

A challenge for the DLL design is that it must lock to frequencies as low as 30 kHz without using a large chip area. The VCDL has 36 stages based on current-starved inverters with low W/L ratio transistors. The charge pump current is 3.5 μ A. It includes a unity gain amplifier that biases the current bypass path to prevent distortion due to charge sharing. The 200 pF loop filter capacitor is integrated on the chip.

4 Retinal Electrode Stimulus

The basic waveform for stimulating human neurons is a biphasic current pulse with charge balance. Early measurements with patients indicate that a maximum current amplitude of 600 μ A is required, and that the electrode impedance is about 10 k Ω . Therefore an output voltage range of more than 12 V is needed. Because the optimal waveform parameters for a retinal prosthesis are not yet known, and because they vary among patients, our stimulator circuit is designed to provide extensive waveform generation flexibility.

The prosthesis chip has twenty current pulse stimulator circuits, each of which implements 4-bit linear amplitude control. The stimulators operate in one of three current ranges, with full-scale currents of 200, 400, and 600 μ A, and LSB increments of 12.5, 25, and 37.5 μ A. A single range for all twenty stimulators is selected during configuration. Each stimulator circuit is connected to five electrodes through a demultiplexor. Implemented in conjunction with the output demultiplexor is a switched bridge circuit that allows a single current source with a single supply to create bipolar pulses. A slightly simplified schematic of the stimulator circuit is shown in Fig. 4.

Each stimulator consists of fifteen parallel current sources. Four data bits in each frame switch 8, 4, 2, and 1 sources. The sources are controlled by switching their gates to the bias voltage or ground. This method avoids the voltage overhead of series switches, and so increases the output voltage range. Because the current output experiences a voltage swing as large as 6 V, we cascoded the current sources to improve output impedance and linearity of current control. The current and cascode bias voltages are created by a wide-swing cascode bias circuit that minimizes the required supply voltage overhead beyond the output voltage range [4]. Two configuration bits select the bias voltages for one of the three current ranges. The stimulus circuit can span the 6 V output range with a 7 V supply.

The control logic block creates clock signals that control the distribution of the input data to the drivers, the timing and polarity of the pulses, and the sequencing of the demultiplexors. The core of the timing logic is an 80-bit ring counter that is clocked by the input data clock. The counter cycles

five times for each image frame, and so the resolution available for controlling the timing of the current pulses is 0.25 % of the frame period. By initializing the state of the counter with two blocks of consecutive ones with particular lengths and positions, we define the widths and interval of the positive and negative pulses. Three overlapping clock signals provide a defined sequence of events to output glitches.

Each demultiplexor is controlled by a 5-stage ring counter which cycles through the five electrodes once per frame. Each counter can be configured so that any of the five electrodes is the first of each frame. Also, the four electrodes not selected are connected to the current return path through weak transmission gates to prevent buildup of local charge in the retinal tissue.

5 Measurement Results

Our prototype device is implemented in a 1.2 μ m CMOS process. The die measures 4.7 mm by 4.6 mm. Its size is constrained by the large number of bonding pads rather than the area of the circuits. Our measurements of the prototype chips show that both the ASK and PWM demodulator circuits can operate at data rates from 30 kbps to more than 1 Mbps. The stimulus circuits can operate at up to 500 image frames per second with a pulse timing resolution of 0.25 percent of the frame period. The maximum power dissipation in the retinal tissue for worst-case image data and pulse widths is 63 mW. Typical values are in the range of 1 to 3 mW. The power consumption in the stimulus chip depends on the image frame rate. For a frame rate of 100 Hz (data rate of 40 kbps) the worst-case overhead power is approximately 3 mW. Fig. 5 shows measured waveforms for the ASK envelope, demodulator output, and recovered data. Fig. 6 shows measured waveforms from three stimulus outputs.

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