A Neuro-Stimulus Chip with Telemetry Unit for Retinal Prosthetic Device

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***Abstract*—In this retinal prosthesis project, a rehabilitative device is designed to replace the functionality of defective photoreceptors in patients suffering from retinitis pigmentosa (RP) and age-related macular degeneration (AMD). The device consists of an extraocular and an intraocular unit. The implantable component receives power and a data signal via a telemetric inductive link between the two units. The extraocular unit includes a video camera and video processing board, a telemetry protocol encoder chip, and an RF amplifier and primary coil. The intraocular unit consists of a secondary coil, a rectifier and regulator, a retinal chip with a telemetry protocol decoder, a stimulus signal generator, and an electrode array. This paper focuses on the design, fabrication, and testing of a microchip which serves as the telemetry protocol decoder and stimulus signal generator. It is fabricated by MOSIS with 1.2-mm CMOS technology and was demonstrated to provide the desired biphasic current stimulus pulses for an array of 100 retinal electrodes at video frame rates.**

***Index Terms*—Biomedical telemetry, neuro-stimulator, retinal prosthesis.**

I. Introduction

OVER 10 000 000 people worldwide are blind because of photoreceptor loss due to degenerative retinal diseases such as age-related macular degeneration (AMD) and retinitis pigmentosa (RP). The retinal prosthesis under development is based on the concept of replacing photoreceptor function with an electronic device. In a healthy retina, the photoreceptors initiate a neural signal in response to light. Photoreceptors are almost completely absent in the retinas of end-stage RP and AMD patients. However, cells to which photoreceptors normally synapse (i.e., the next neuron in the signal path) survive at high rates [1]. Previous clinical studies have shown that controlled electrical signals applied to a small area of the retina with a microelectrode can be used to initiate a local neural response in the remaining retinal cells [1]–[7]. The neural response was perceived by otherwise completely blind patients as a small localized phosphene, or spot of light. When multiple electrodes were activated in a two-dimensional electrode array, a number of phosphenes are perceived by the patient which when viewed together form an image representative of the pattern of active electrodes. In the experiments reported by Humayun [1], simple forms such as an English character or a matchbox have been perceived by human subjects when the corresponding pattern electrical stimulation of the retina is given. When controlled pattern electrical stimulation of the remaining retinal neurons is driven by an extraocular image acquisition and transmission system, it could allow blind patients to regain form vision of their environment, or of a computer-generated image. The conceptual design of the system is illustrated in Fig. 1.

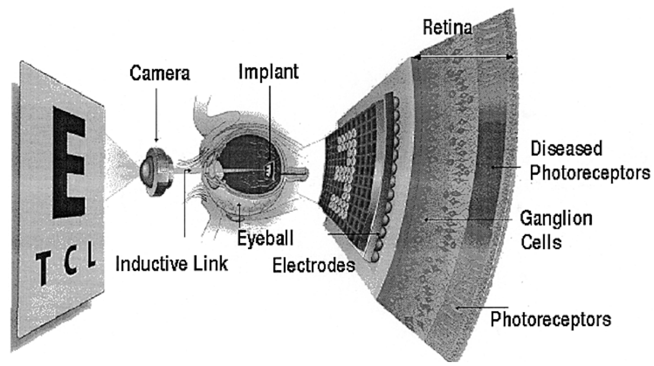

Fig. 1. Retinal prosthesis system.

The required waveform of the electrical stimulus is characterized by four parameters (amplitude, width, interphase delay, and frequency) and is shown in Fig. 2. A waveform could be either an anodic pulse first followed by a cathodic pulse or vice versa only if an equal amount of charge is provided by both anodic and cathodic pulses in order to obtain a balanced charge. It has been determined that the preferable stimulus waveform is the one with a leading cathode pulse [1]. Depending on the degree of damage in a patient's retina, the medical doctor must be able to finely tune these four parameters accordingly via telemetry protocol specification once the device is implanted.

Medical experiments have estimated that the equivalent impedance for the retina tissue of RP and AMD patients is about 10 kΩ and, in the worst case, the current threshold value is about 600 μA [1]. Thus, a voltage drop up to 6 V is expected across the retinal tissue. In addition, the prosthetic device must dissipate as little power as possible since it resides in the

Manuscript received August 31, 1999; revised June 29, 2000. This work was supported in part by the National Science Foundation under Grant BES-9509758 and Grant BES-9808040.

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Publisher Item Identifier S 0018-9200(00)08710-2.

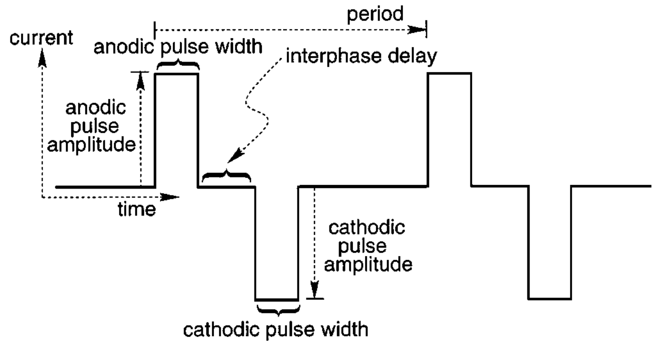

Fig. 2. Electrode current stimulus waveform.

eyeball. In the literature, several fine neuro-stimulator devices have been proposed [8]–[10]. However, they are not applicable to our retinal prosthesis application.

Previously, we developed a visual intraocular prosthesis chip including a photosensor, processor, and stimulus-driving chip for a 5×5 electrode array [11]. The chip was capable of delivering the requisite currents for retinal stimulation in humans, as was determined by clinical studies conducted on visually impaired patients with RP and AMD. However, it became apparent that an improvement could be achieved in having the photosensing or video capture performed extraocularly, allowing for enhanced video-processing, more custom control over the video signal, and less hardware to be implanted into the eye. Currently, we are developing the prosthesis system which is conceptually illustrated in Fig. 1. The system is composed of two units, one extraocular and one intraocular. The two units are connected by a telemetric inductive link, allowing the intraocular unit to derive both power and a data signal from the extraocular unit. The extraocular unit includes a video camera and video processing board, a telemetry protocol encoder chip, and an RF amplifier and primary coil. The intraocular unit consists of a secondary coil, a rectifier and regulator, a retinal stimulator with a telemetry protocol decoder and stimulus signal generator, and an electrode array. The system block diagram is shown in Fig. 3.

After receiving visual information from a video camera, the extraocular unit provides additional image processing whose output is further encoded with a specific data transmission protocol which is described in Section II-A.1–A.2. Two types of data, configuration and image, are distinguished by bit patterns in the transmission protocol. The data is further processed by a pulse width modulation circuit (PWM) and subsequently modulated onto an RF carrier using amplitude shift keying (ASK). The modulated carrier is then inductively transmitted to the intraocular unit. The PWM data signal and power carrier in the received signal are then separated by a filter in the intraocular unit. The filter design dictates the ratio of carrier frequency to the data rate. In our design, the data rate can be 25–250 kb/s with 1–10-MHz carrier dc power is obtained from the carrier by rectifier and regulation and must be independent of the data stream. Our PWM scheme is designed to achieve such a stringent power requirement. Either configuration or image data is extracted through the reversal process of the encoding which was applied by the extraocular unit. In other words, configuration/image data is extracted from the digital PWM signal and is used as a specification for the generation of the current pulses. In turn, these current pulses drive the electrode array.

Research pertaining to all of the component blocks in Fig. 3 is underway. In this paper, we describe the design and testing of the component chip referred to as the "implanted stimulator" in Fig. 3. The chip accommodates the telemetry function, protocol receiver, and stimulus current drivers. It serves as a flexible current waveform generator and could potentially obtain the optimization of stimulus waveforms via implant experiments. It supports the charge-balanced current with a biphasic waveform (anodic phase first followed by a cathodic phase) as shown in Fig. 2. It is also capable of providing the wireless transfer of power and data to the implanted stimulator.

The paper is organized into five sections. The prototyping chip is presented in Section II with discussions of stimulator functionality and operation and circuit design issues. Section III presents the measurement results of the chip. Section IV summarizes device limitation and offers possible methods and means of improvement, followed by the conclusion in Section V.

II. Implantable Retinal Chip

A. Chip Functionality

Referring to the block diagram of the implanted stimulator in Fig. 3, the chip operates in two modes, configuration and run (imaging) mode. The ASK demodulator receives the power-carrier envelope from the rectifier output and generates the digital PWM signal for the clock and data recovery block. Data and clock signals are then recovered by a delay-locked loop (DLL) and a decoder circuit. The chip enters the configuration mode after locating a synchronization word in the the data stream using a sync detector circuit. As discussed in Section II-A.4, a configuration frame has 400 bits and consists of two fields, "syncword" and "configuration data" fields. In this mode, according to the configuration data, the timing generator circuit is programmed to produce the timing of the stimulus waveforms, including the anodic/cathodic pulse widths, the interphase delay, and the biphasic pulse period. The current control circuit specifies the full-scale amplitude of biphasic current pulses. This specification is then applied to each of the 20 stimulus current drivers; each drives five electrodes through demultiplexing. Once the configuration process is completed, the chip automatically enters the run mode. By multiplexing, the 20 electrode stimulators drive the desired biphasic current pulses to the 10×10 electrode array.

1) ASK Demodulator: The prototype implantable device receives both power and data via an inductive link. Amplitude modulation instead of frequency modulation is chosen in order to reduce the circuit complexity and power consumption and is able to sustain the data rate of the requisite functions. The ASK modulation scheme governs the amplitude of the carrier signal according to the desired digital data. Because the recovered power is also derived from this amplitude, the average transferred power could depend on the transmitted digital data pattern. To avoid this data dependency, we first encode the data to be transmitted using the alternate mark inversion PWM scheme which subsequently modulates the power carrier. The system is

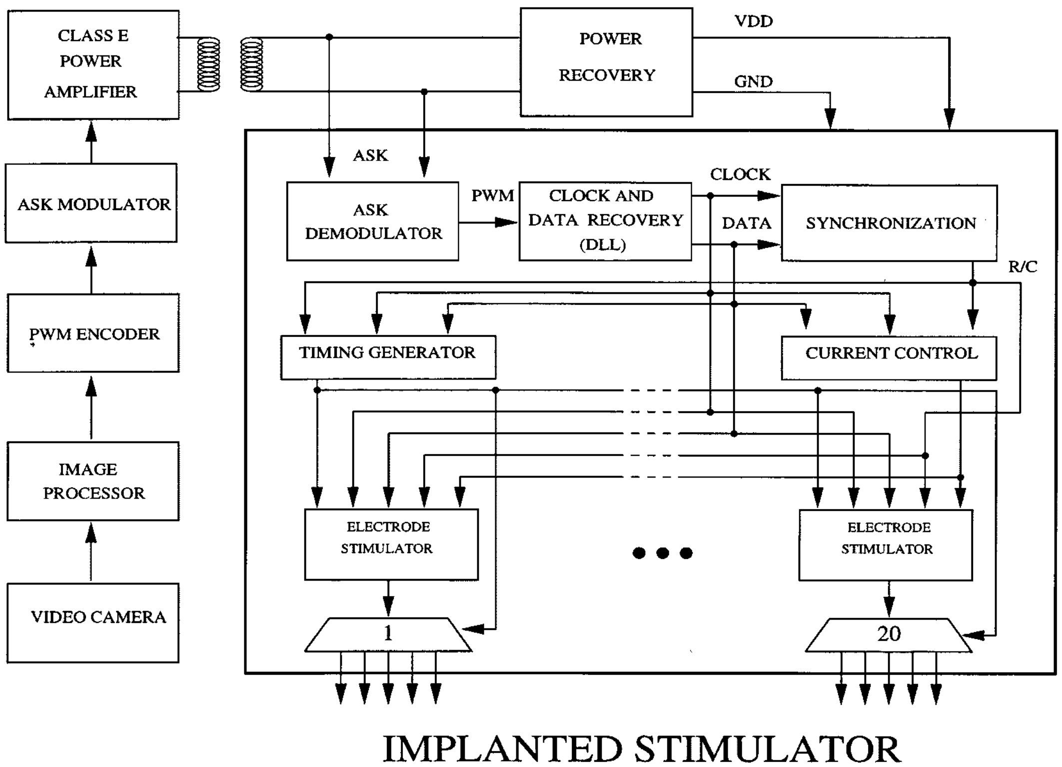

Fig. 3. System block diagram for the proposed retinal prosthetic device.

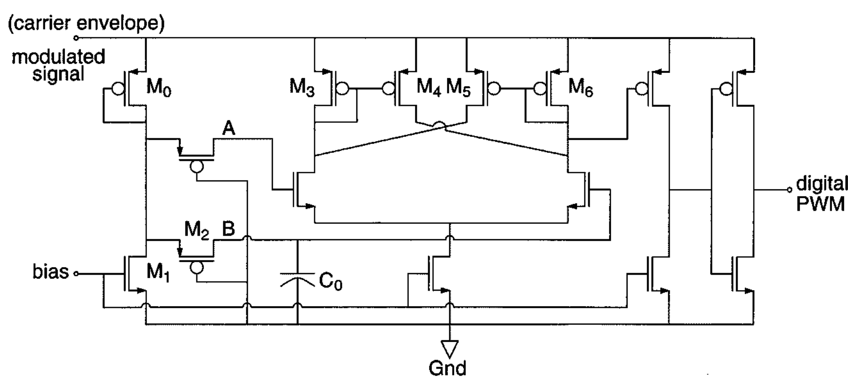

Fig. 4. ASK demodulator circuit.

designed for PWM data ranging from 25 to 250 kb/s with a carrier frequency ranging from 1 to 10 MHz.

On the receiver side, the power carrier is rectified and filtered to obtain the baseband carrier envelope containing the PWM data. The envelope is further filtered in order to provide a low-ripple dc voltage for the chip power supply. The unfiltered carrier envelope is passed to the ASK demodulator circuit of Fig. 4 to extract the digital (rail-to-rail) PWM waveform.

The demodulator is a comparator with a predefined amount of hysteresis in which one input is derived from the envelope of the modulated carrier, labeled "A" in Fig. 4. The other input is derived from the average of that signal, labeled "B" in Fig. 4 [12]. Transistors M_0 and M_1 provide level shift of the input signal to the common-mode range of the differential amplifier. Transistor M_2 and the 10-pF capacitor C_0 serve as a low-pass filter and provide the average of an input signal. Both signals are applied to the differential amplifier with the cross-connected active load of M_3–M_6. The hysteresis is achieved via positive feedback. The demodulator is designed to process the carrier envelope with a ripple between 6.5 to 7.5 V. It has a hysteresis of 500 mV, so as to ensure that the likelihood of an extra transition in the output waveform due to noise is minimized. The output waveform of the demodulator is the digital PWM with voltage swing between 0 and 7 V.

2) Clock and Data Recovery Circuit: The rising edges of the PWM signal from the demodulator are fixed in time periodically and serve as a reference in the derivation of an explicit clock signal. On the other hand, the data is encoded by the position of the falling transition at each pulse. In an alternate mark inversion encoding scheme, a zero is encoded as a 50% duty cycle pulse, and ones are alternately encoded by 40 or 60% duty cycle pulses. This eliminates the need for a local clock oscillator such that the clock and data recovery circuit is simplified. It also provides an average coupled power which is essentially independent of the data.

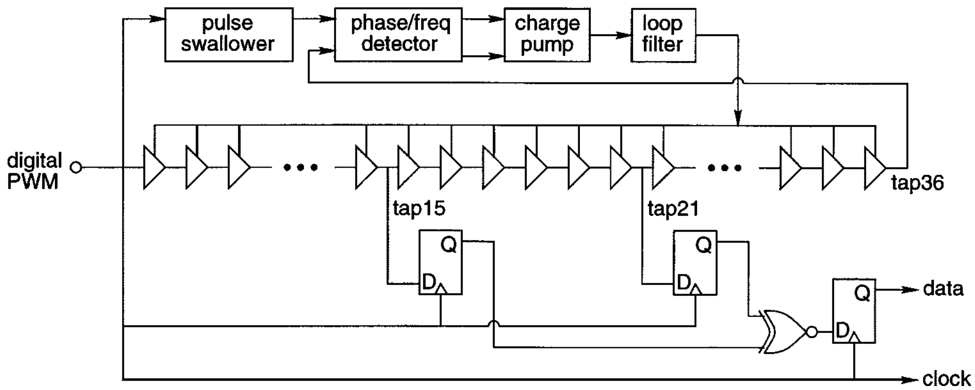

Fig. 5. Clock and data recovery.

The diagram of the clock and data recovery unit is shown in Fig. 5. It consists of a DLL and decoder logic. The DLL consists of a phase-frequency detector (PFD), a charge pump, a loop filter, and a voltage-controlled delay line. The 36-stage delay line is locked to one period of the PWM waveform. The waveform is decoded by an XNOR gate whose inputs are the tapped-out signals at the fifteenth and twenty-first stages. The positions for the tapped signals correspond to the duty cycle percentages used in the PWM waveform.

A challenge for the DLL design is to make the lockable frequency as low as 25 kHz without consuming a large chip area. A three-state PFD is used with the additional delay at the reset path to reduce the dead-zone effect. The voltage-controlled delay line is based on current-starved inverters made of low W/L transistors. The charge-pump current is 3.5 μA provided by matched wide-swing current sources. A unity gain amplifier is included to prevent the ripple distortion of the control voltage due to charge sharing. The 200-pF loop filter capacitor is integrated on the chip. The initial condition of the DLL must be set correctly to guarantee a correct locking condition. The very first input to the PFD after reset must be the rising edge of the PWM waveform *fed back from the delay line*. This can be enforced by using a simple pulse-swallow circuit which would only ignore the very first pulse of the *incoming PWM waveform* prior to entering the PFD. The loop filter capacitor is initialized to full charge when power is applied. Consequently, the delay line starts with the smallest delay. The loop then initiates the discharge of the capacitor resulting in a decrease of the control voltage and an increase of the delay. This process continues until the delay is exactly equal to one period of the incoming PWM waveform. In this way, locking to a subharmonic of the PWM waveform is prevented. The DLL is always stable since it is a first-order system.

3) Synchronization Circuit: The synchronization circuit facilitates the transitions of the device from the *power-on state* through the *configuration state* to the *stimulus state*. It contains an 8-bit synchronization word detector circuit and an 8-bit counter, as shown in Fig. 6. Once the DLL begins producing the clock and data signals, the synchronization circuit examines the data until it detects the predefined 8-bit sync word that defines the beginning of the configuration state. This state lasts for 256 clock periods. After 256 clock cycles, the sync circuit activates the run/configure (R/C) signal and the chip enters the run (stimulus) state.

4) Timing Generator and Current Control Circuit: The timing of the stimulus pulse for all of the current drivers is centrally controlled, and is specified in integer multiples of the master clock period. The timing control circuit contains 20 of 5-bit control first-in-first-outs (FIFOs), an 80-bit timing FIFO, and combinational logic. The current control circuit is a 2-bit current reference register and a bias generator circuit. The overall circuit diagram is shown in Fig. 7. When the sync detector circuit locates the synchronization word and de-asserts the R/C signal to indicate the configuration mode, all the switches in Fig. 7 are set to the C (configure) position. Thus, the 20 of five-stage ring counters, the 80-stage ring counter, and the 2-bit reference current register are connected together as a single 182-stage FIFO. The FIFO is strobed by the recovered master clock for 256 cycles, during which time the FIFO serially shifts in recovered data. The last 182 bits are retained while the first 74 bits are shifted through and discarded. The 182-bit data contains three fields. The first two bits define the amplitude of the full-scale output current. The next 80 bits define the current pulse timing (anodic/cathodic pulse widths and interphase delay), and the last 100 bits define the firing sequences of the electrodes driven by each current driver demultiplexer. Each current driver controls a group of five electrodes; the firing sequence for the group is specified by a five-stage ring counter. When the count of 256 clock periods is reached and flagged by the synchronization circuit, the R/C signal is asserted and the switches are set to the R (run) position. The chip remains in this state until an external reset is applied or until power is removed. The 182-bit FIFO is then regrouped as 20 of 5-bit control FIFOs, an 80-bit timing ring counter, and a 2-bit bias register. The chip is then ready to activate the stimulation mode. The image data is loaded into 20 of 4-bit data FIFOs (overall it has 80 bits). The amplitude of each current driver is established by the value within the corresponding 4-bit data FIFO.

According to the 2-bit reference current register, a maximum current amplitude of 200, 400, or 600 μA for the wide-swing current source [13] is selected. A finer resolution could be obtained by the specification of the 4-bit data FIFO. The 80-bit ring counter is loaded with two blocks of consecutive ones which specify the width of the anodic and cathodic pulses and also the interpulse interval (dead time). During the stimulus state, the two blocks cycle through the counter five times per

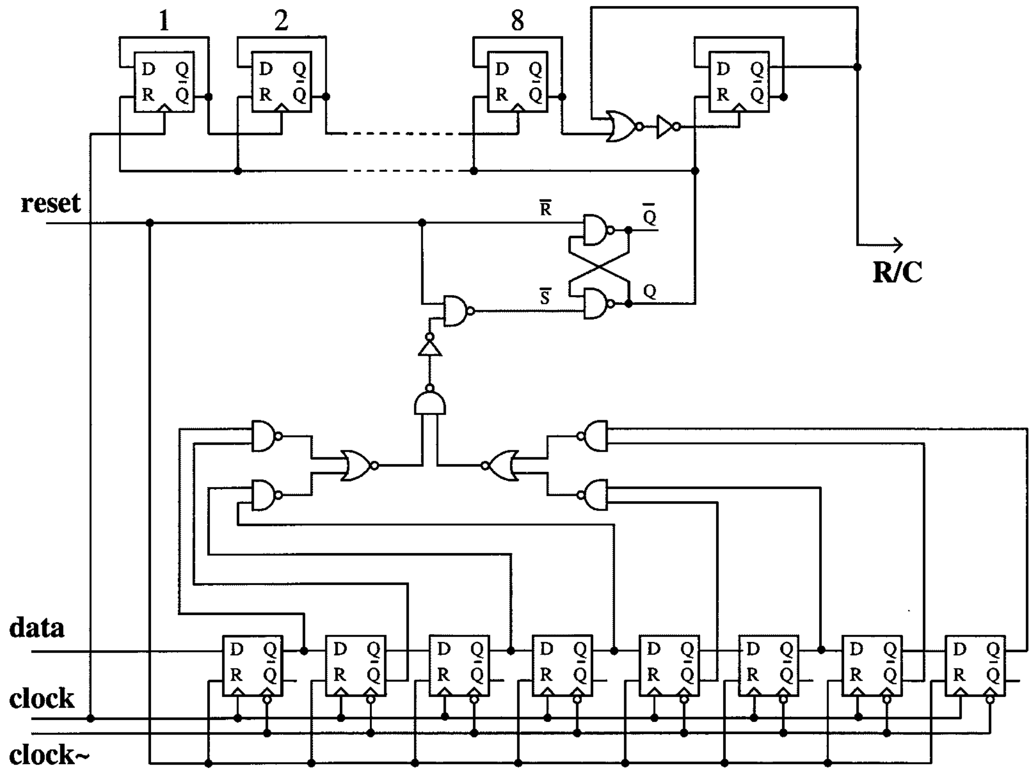

Fig. 6. Synchronization circuit.

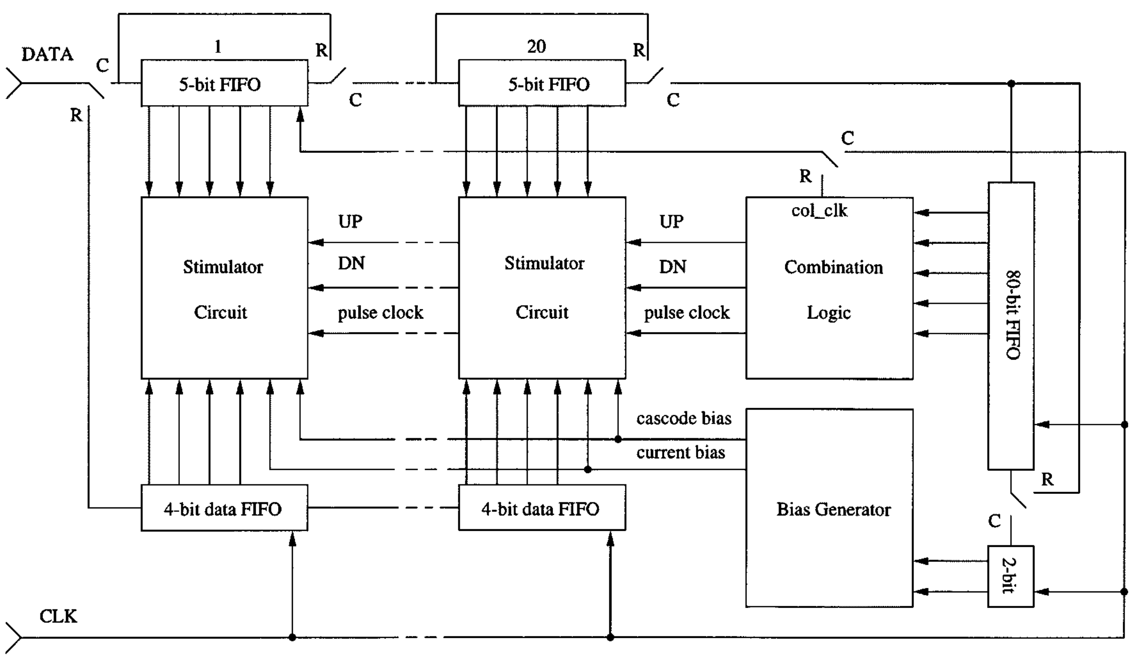

Fig. 7. Timing generator circuit.

frame. The times that the block sweep past five particular counter tabs define the timing of the anodic and cathodic current pulse through the UP and DN signal generated by the combination logic. This provides the resolution for controlling the pulse-width timing to be 1/400 frame. The associated logic produces COL_CLK for the 20 of 5-bit ring counters that no longer use the master clock after entering the stimulus state and $PULSE\_CLK$ used together with the image data to switch current sources between the bias voltage and GND in the stimulator circuits. Each 5-bit ring counter is loaded with a single one, and each controls the current demultiplexor by cycling through the five electrodes once per frame. Each counter can be configured so that any of the five electrodes is the first of each frame.

5) Current Pulse Stimulator Circuit: There are 20 pulse-stimulator circuits in the chip, all of which support a set of

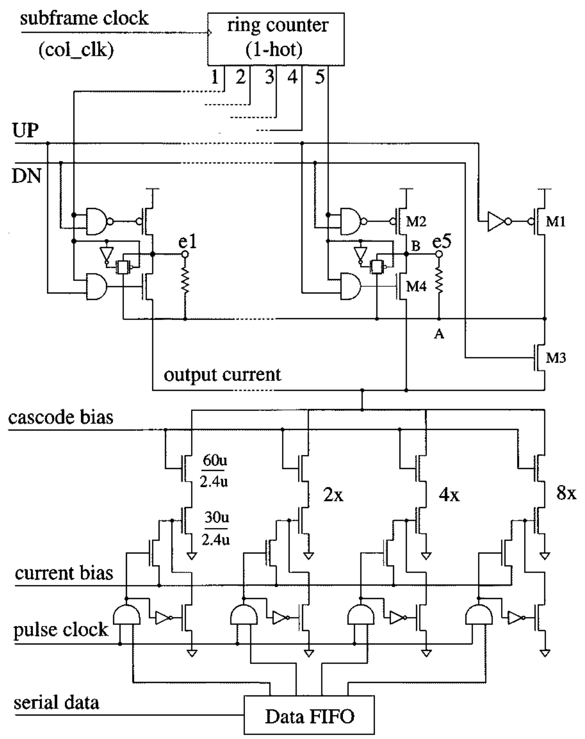

Fig. 8. Stimulator circuit.

full-scale current value of 200, 400, or 600 μA. The current at each stimulator can be refined by the corresponding image data with 4-bit resolution. In our implementation, this single full-scale current value applies to all 20 stimulators and is specified during configuration. The stimulator circuit is illustrated in Fig. 8. The stimulator is based on a 4-bit binary-weighted digital-to-analog converter (DAC), and thus consists of 15 parallel current sources. For each binary-weighted current source within the DAC, the corresponding data bit specifies that the associated gate potential be switched either to the bias voltage (for conduction) or to ground (for cutoff). This method avoids the voltage overhead of series switching, thereby increasing the output voltage range. Due to the 10 kΩ tissue impedance, the electrode experiences a voltage swing as large as 6 V per phase. The biases for the current source and cascode field-effect transistors (FETs) at the selected current range are provided by a wide-swing cascode bias circuit such that the required supply-voltage overhead is minimized. The stimulus circuit can accommodate the 6-V output range with a 7-V supply. Cascode devices also improve the output impedance and linearity of control.

Directly sourcing and sinking current to synthesize biphasic stimulus output requires dual supply rails of $+7$ V and -7 V, as well as sourcing and sinking current sources. A switched bridge circuit was designed to create a biphasic current pulse from a single current source with a 7-V supply. It is implemented as part of the output demultiplexer and allows the electrodes to be connected to the stimulator with either polarity. Each demultiplexer is sequenced by a 5-stage ring counter which cycles through the five electrodes once per data (image) frame. To create a biphasic current pulse at "e5," for example, the fifth tap of the ring counter would be activated. The UP signal enages M_1, M_4 while M_2, M_3 remain off, allowing current to flow from A to B as an anodic pulse. Then the DN signal engages M_2, M_3 while M_1, M_4 are off, allowing current to flow from B to A, creating a cathodic pulse. The other four nonselected electrodes are connected to the current return potential through weak transmission gates to prevent the buildup of local charge in the retinal tissue.

6) Biasing Circuit: The biasing circuit is shown in Fig. 9. It is a threshold-voltage-referenced self-biased circuit [14]. The voltage reference is established from the intersection of the linear voltage–current relationship of R_1 (50 kΩ resistance) and the quadratic voltage–current relationship of nMOS transistor M_1. This gives a voltage reference independent of supply-voltage variation due primarily to fluctuation in inductive coupling associated with movement of the eyeballs.

Although the threshold voltage of the nMOS transistor is temperature dependent, it would not significantly affect the circuit, since the chip temperature is kept relatively constant and close to the body temperature. The drawback of this circuit, however, lies in the difficulty of fabricating precise resistance in CMOS technology. However the remedy can be done as suggested in Section IV.

The current of the biasing circuit is mirrored to six identical cascode transistors to form a reference current. The 2-bit bias voltage register engages either two, four, or six cascode transistors, resulting in three reference current levels. The reference current flows through diode connected transistors in the wide-swing topology to produce bias voltages for current sources in the stimulator circuits.

III. Measurement Results

The prototype device was implemented in 1.2-mm CMOS technology. The die size is 4.7 $\times$4.6 mm^2. The minimum size is determined by the large number of bonding pads rather than the area of the circuits. The chip is designed such that it can be tested as a complete system or as separate subsystems.

A. Communication Circuit

The chip is designed only to receive externally initiated communication; no back-telemetry is implemented. Although intended for a data rate of 25 to 250 kb/s, our measurements show that the ASK and PWM demodulator circuits can operate in excess of 1 Mb/s. However, at this high data rate, the modulation index needs to be increased up to 30% due to the reduction of the amplifier gain. Fig. 10 shows the measured communication waveforms. Channel1 is the carrier envelope (top waveform), channel2 is the PWM output from the demodulator, and channel3 is the recovered nonreturn to zero (NRZ) data. Note that there are two clock periods of latency between the NRZ output and the PWM input, owing to the flip-flops in Fig. 5.

B. Stimulator Circuit

As described earlier, the stimulator circuit is capable of delivering the three full-scale current ranges of 200, 400, or 600 mA through a 10-kΩ resistive load. Within each range, there is 4-bit linear resolution or 16 different levels. Consequently, the current range can be selected appropriately for individual patients

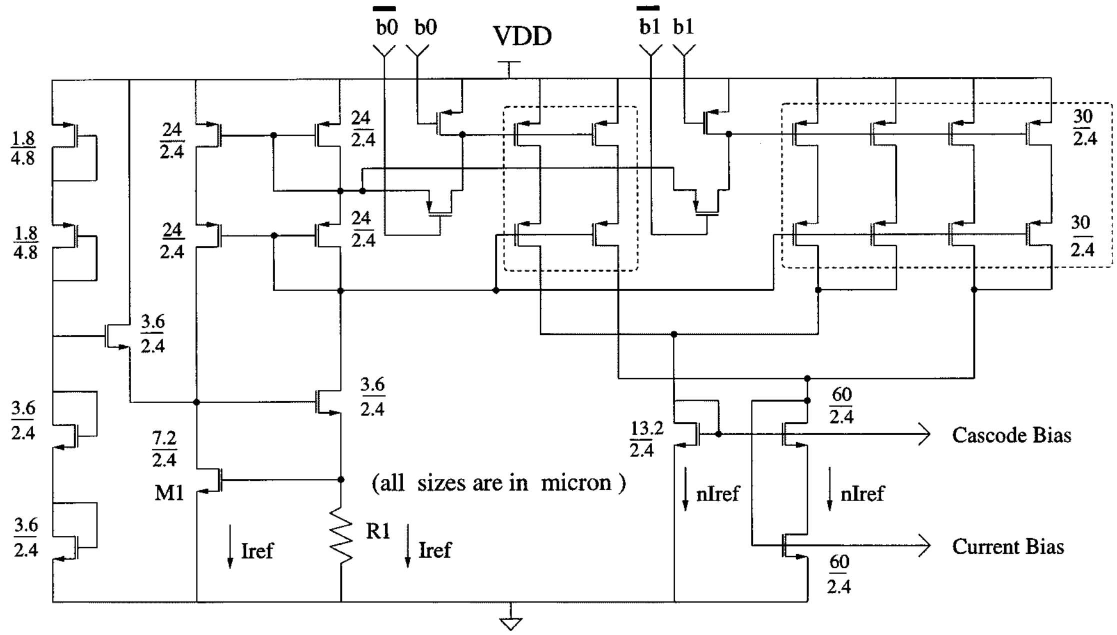

Fig. 9. Bias generator circuit.

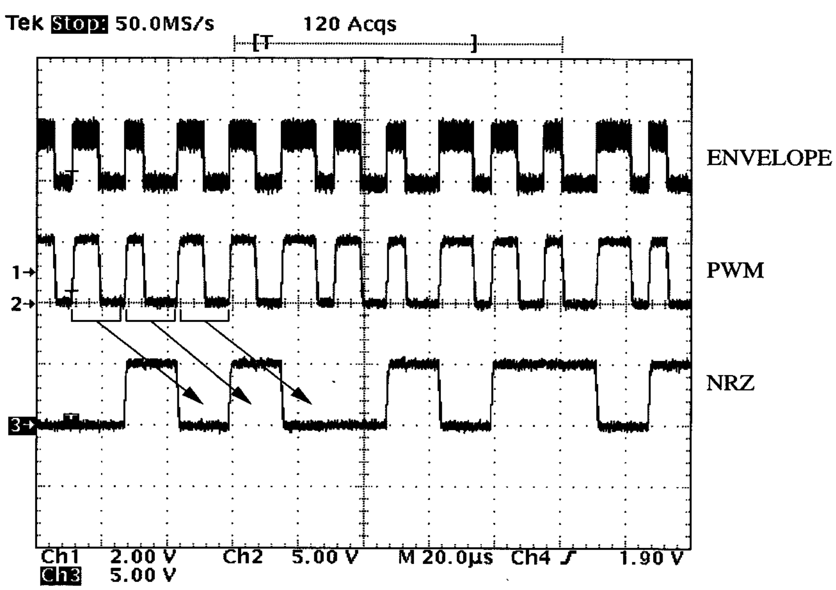

Fig. 10. Measured communication waveforms.

in clinical testing. The ability to produce accurate charge-balanced biphasic current pulses is of major concern. We characterize the performance of the stimulator circuit in terms of accuracy, linearity, and power supply sensitivity (the sensitivity to random variations in the inductive link, due to relative motion between the coils).

1) Accuracy: We measured the current output at the nominal 7-V supply with a resistive load of 10 kΩ. The results show that both anodic and cathodic amplitudes are smaller than the nominal value in all three full scales. This apparently results from a decreased reference current. This is mirrored from the biasing current which in turn depends on the resistor in the bias generator circuit. In this case, process variation makes resistance greater than the design value. The matching between anodic and cathodic amplitudes is acceptable, as the mismatch error is less than 5%. With the built-in charge neutralizer switch at every electrode, any accumulated charge on an electrode can be quickly depleted. Example output waveforms are shown in Fig. 11, composed of 15 stimulus waveforms from three output drivers exciting five different amplitudes, repectively.

2) Linearity: In Fig. 12, we plot the output current amplitude verses DAC digital input for each full-scale current setting. Although the amplitude is smaller than the designed value, the DAC returns reasonable linearity in all scales. A linear DAC transfer function facilitates characterizing visual perception with respect to stimulus current amplitude.

3) Power Supply Sensitivity: The variation of inductive coupling can affect the stimulator circuit in two different ways. First, there is a direct change in the power-supply voltage, which impacts the drain-to-source voltages V_{DS} of the current sources.

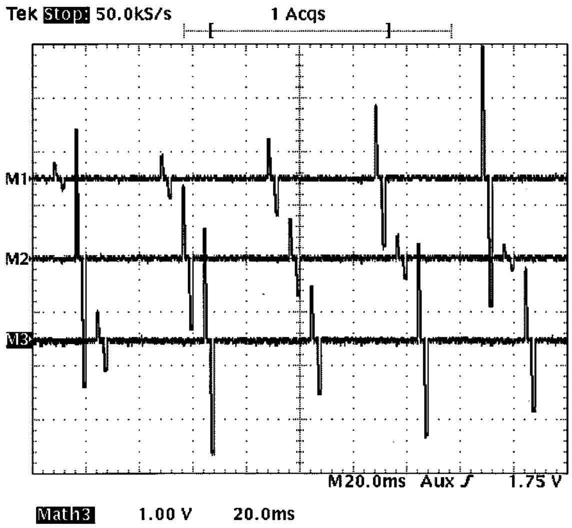

Fig. 11. Measured stimulus waveforms.

This effect contributes the same result as a variation in the load impedance (retinal tissue) from one patient to another patient. It may be alleviated by designing the current sources with a high output impedance. In our design, we use wide-swing cascode current sources which provide an output impedance in excess of 2 MΩ.

The second effect comes indirectly through the bias generator circuit. A shift in supply voltage can cause bias variation which changes the gate-to-source voltages V_{GS} of the current sources. The solution to eliminating this fluctuation is to use a biasing circuit that is less sensitive to supply variation. This is verified by varying the supply voltage from 6 to 9 V and measuring the output current. A plot of the three full-scale output currents as a function of supply voltage is shown in Fig. 13. The current amplitude is almost independent from supply voltage. The variation of amplitude over the range is less than 10%. Clearly, the circuit is able to maintain the acceptable current amplitude.

4) Power Consumption: The total power consumption of the device is contributed from two sources, namely the power consumption of the stimulus chip itself and the power dissipated into the load (retinal tissue). The power consumption in the stimulus chip depends on the image frame rate. In our application, the frame rate is greater than 60 frames/s [1]. The power dissipation at 100 frames/s, corresponding to a data rate of 40 kb/s, would be approximately 3 mW.

Additional power consumption for the prosthesis is associated with the wireless inductive link. It depends on several factors such as carrier frequency, coil geometry, coil-separation, number of turns, angular alignment, and choice of amplifier [15]–[18]. Most of these are subject to variation in prostheses. For example, Ziaie reported that additional 300–400 mW was consumed in the inductive link [19].

Depending on the pulse amplitude and the ratio of a pulse width to a frame period, the average power dissipation at the load impedance is calculated as an average power of a biphasic pulse period by the following:

$$P = NAI^2 = NRA^2W/400$$

where

- N number of driven electrodes;
- R tissue equivalent impedance;
- I average current for each electrode during the observation period;
- A pulse amplitude;
- W pulse width in clock periods.

There are 400 clock periods per frame.

For the worst-case scenario, all 100 electrodes are driven with the full 600 μA amplitude with anodic and cathodic pulse widths of 25 clock-period duration (corresponding to one-eighth of a stimulation period when accounting for both anodic and cathodic phases). When driving 100 loads of 10 kΩ each, this gives an average power of 5.6 mW. This is the case that the highest power is dissipated by the chip, however, it is unrealistic that all electrodes would be simultaneously fired.

A statistical assumption of stimulus pulses operating at half maximum amplitude over half of the worst-case anticipated pulse duration would account for 25% of this average power, or 1.4 mW. When added to the previous 3 mW associated with the stimulator circuits, this accounts for intraocular power dissipation on the order of 5 mW. The prototype device characteristics are summarized in Table I. The die micrograph is shown in Fig. 14.

IV. Design Enhancements

The prototype chip behaved according to its design specifications, except for a small degradation of the current amplitude due to process variations. The communication circuit operates in a wide range of data rates up to 1 Mb/s. This data rate is capable of supporting a 64 × 64 electrode array at 60 frames/s. Because of the fragility of the retina, the stimulator IC will not directly contact the retina, but rather a flexible substrate (e.g., polyimide) electrode array will be connected to the stimulator and routed to the area of interest on the retinal surface. A number of factors might limit the number of achievable electrodes, such as availability of bond pads on the stimulator (particularly if a pad ring is used) or the number of electrodes imprintable on a flexible substrate (at a typical diameter of 400 mm and 200 mm pitch) [1], [20]. However, the likely limiting factor of spatial resolution will be the number of connecting traces which can be routed along the length of the array. A maximum electrode count on the order of 200–300 is expected with this connecting topology. The minimum number of electrodes needed to provide useful vision has not been determined via a functioning prototype as of this date. Nevertheless, the ability to support a wide range of data rates allows for clinical testing with biphasic stimulating pulses at different frequencies and amplitudes, leading to a more detailed characterization of the relationship between visual perception and stimulation waveforms.

The current amplitude is smaller than the designed value, because there is a mismatch between the fabricated and simulated resistance value in the bias generator circuit as previously described. This type of biasing circuit is susceptible to resistance deviations due to process variation. In our case, rather than the absolute value, it is more critical to have the ability of generating

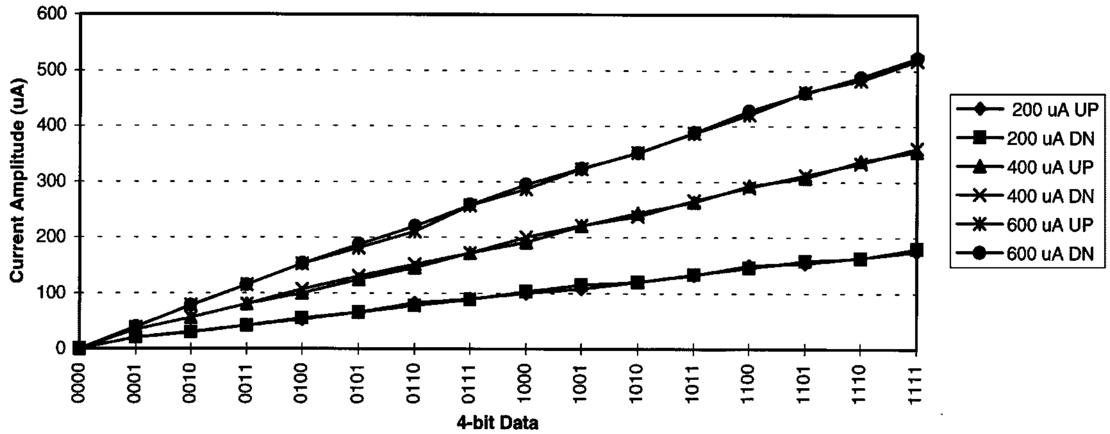

Fig. 12. DAC linearity.

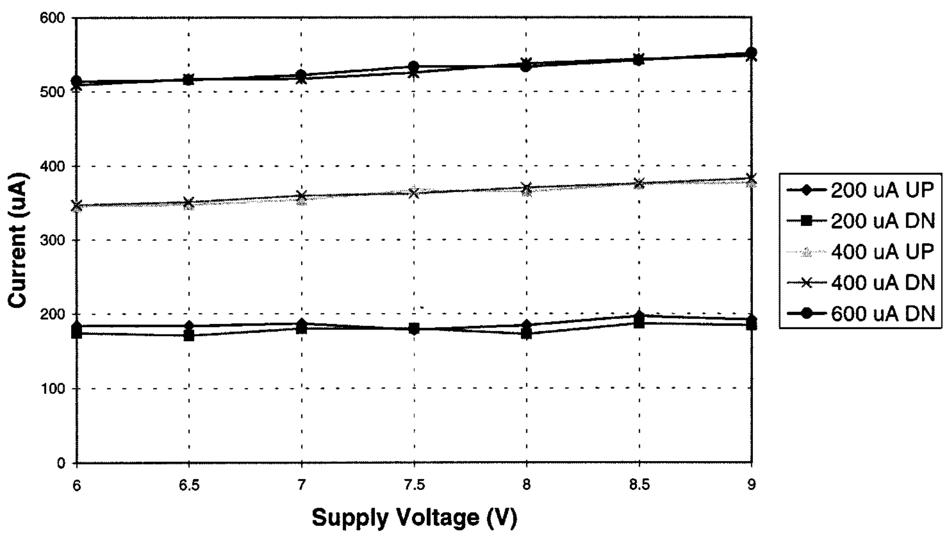

Fig. 13. Full-scale output current as a function of supply voltage.

TABLE I
CHIP PERFORMANCE SPECIFICATION AND THE MEASUREMENT RESULT

Technology	MOSIS's CMOS 1.2 mm
Die size	4.7mm x 4.6 mm
Carrier frequency	1-10 MHz
Number of current generators	20
Number of electrodes	100 (10 x 10 array configuration)
Data rate	25 kbps-250kbps[1]
Maximum frame rate	600 frame/sec
Amplitude resolution	4-bit, 3 full-scale
Timing resolution	1/400 of frame period
Power consumption	5 mW @ 7 V and 100 frame/sec
Frame size (configuration and image data)	400 bits

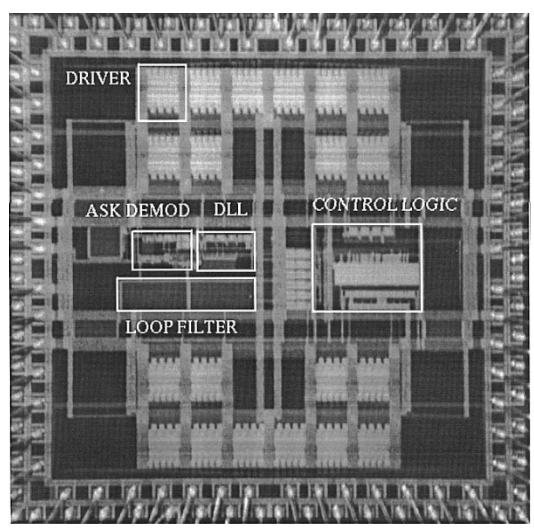

Fig. 14. Die micrograph.

a voltage reference which is less sensitive to supply voltage variation. In general, there is a 20% variation of the resistance value due to process variation. However, in practice there are two ways to correct this if the variation is beyond the tolerance. One is by trimming the resistors after fabrication by using the focused ion beam (FIB) technique. An alternative is to design a set of resistors that can be externally programmed. Both methods may provide the desired resistor value.

This chip uses a simple synchronous protocol and timing control. After the chip is configured and enters the run mode, it continues to stimulate until it receives an external reset. This scheme requires only digital circuits with a small number of registers, making the chip design less complex with reduced power consumption. With more detailed logic design and on-chip memory, additional features may be included such as real-time reconfiguration, arbitrary pulse mode, and bidirectional communication.

A. Real-Time Reconfiguration

This facilitates an on-the-fly change in configuration, such as in timing, frame rate, or full-scale pulse amplitudes while remaining in the stimulation mode. This offers the benefit of improving patient feedback to various stimuli in a more real-time manner.

B. Arbitrary Pulse Mode

Currently, the anodic pulse and cathodic pulse of a biphasic pulse are equal in both pulse duration and current amplitude. However, with an arbitrary pulse mode, both anodic and cathodic pulses can be different in amplitude or duration, provided that they balance in charge. Furthermore, stimulus waveforms other than square pulses may be considered.

C. Bidirectional Communication

In clinical testing, the patient can provide verbal feedback regarding the effectiveness of stimulation. As an alternative or supplement, the device itself might offer additional diagnostic information such as electrode status and retinal impedance by measuring the electrical signal at the electrodes and transmitting this information back as serial data to the primary side. Because this upstream data is of low content, the transmission can be a simple impedance modulation scheme. This is based on the principle that a change in the impedance of the resonated secondary coil and associated power recovery circuits can change the effective impedance of the primary side [21]. Alternatively, an active transmitter can be integrated with an on-chip spiral inductor operating as the transmitter coil [22]. These back-telemetry schemes are challenging to design as they must coexist free of interference with simultaneous forward data telemetry.

V. Conclusion

A prototype telemetry/stimulus chip, a core component for a retinal prosthesis system, has been designed, fabricated, and tested. This device is essential in supporting a proposed retinal prosthetic prototype system consisting of extraocular and intraocular units. Data and power transfer between these two units are accomplished via inductive coupling. Special techniques have been applied to prevent the fluctuation of the derived dc voltage. ASK modulation with PWM encoded digital data is used such that the derived dc power from the carrier frequency is independent of the transmitted data content. An on-chip voltage compensation technique is also used to minimize the effect of power supply voltage fluctuation. Hysteresis of 500 mV is included in the ASK demodulator so that configuration/image data can be reliably recovered. The chip is capable of recovering data and power and delivering a flexible stimulus waveform. The device has been fabricated in the AMI 1.2-μm CMOS process through MOSIS. Test results show that the device performs as designed.

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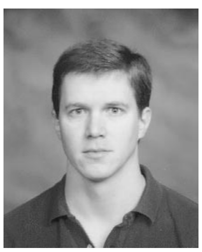

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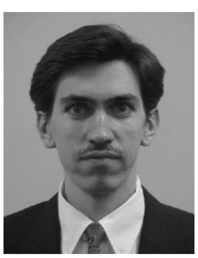

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